RCA Review

March 1976

Volume 37 No. 1

RCARCI 37(1) 1–156(1976)

RCA Review, published quarterly in March, June, September and December by RCA Research and Engineering, RCA Corporation, Princeton, New Jersey 08540. Entered as second class matter July 3, 1950 under the Act of March 3, 1879. Second-class postage paid at Princeton, New Jersey, and at additional mailing offices. Effective Jan. 1, 1971, subscription rates as follows: United States and Canada: one year $6.00, two years $10.50, three years $13.50; in other countries, one year $6.40, two years $11.30, three years $14.70. Single copies (except for special issues) up to five years old $3.00.

RCA Review

A technical journal published quarterly by RCA Research and Engineering in cooperation with the subsidiaries and divisions of RCA.

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CVD Glass Films for Passivation of Silicon Devices: Preparation, Composition, and Stress Properties*

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Abstract—Results of studies are described for successful glass passivation, by chemical vapor deposition (CVD), of metallized silicon planar integrated circuits. The effects of various process conditions for low-temperature (350° to 450°C) CVD of phosphosilicate glass layers by oxidation of silane plus phosphine were systematically correlated with the chemical composition and intrinsic stress properties of deposited films. A practical method has been developed and applied for measuring stress in CVD films deposited on silicon wafers; it requires no special fixtures during deposition and is thus applicable for any type of deposition system. A correlation has been demonstrated between intrinsic stress in deposited films and susceptibility to cracking during deposition or during subsequent exposure to thermal stress conditions, particularly at processing temperatures higher than the deposition temperature. Low phosphorus content in deposited films was correlated with excessive intrinsic tensile stress leading to crack formation. CVD conditions were established for attaining low stress films, and a new technique was devised for achieving further reduction in intrinsic tensile stress of CVD films based on the introduction of water vapor in the reaction chamber during film formation. Finally, the causes of structural defects in CVD glass layer are critically reviewed, and some experimental results on photolithographically induced defects are presented.

1. Introduction

The terms "glassing" and "glass passivation" are commonly used to denote the process in which a glass-like, amorphous, inorganic dielectric layer is formed over the surface of a completed microcircuit wafer

* This work was in part supported by the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-74-C-5146. Portions of this paper were presented verbally at NAECON '75, and an extended summary was included in the proceedings volume.

for the purpose of protection against the ambient. The sequence for glass passivation consists of deposition of the dielectric layer over the entire surface of the device wafer with completed metallization patterns, followed by photolithographic delineation to remove glass from the central region of bonding pads and from scribe line areas. Typical deposited films are 0.5 to 2 μm thick.

The majority of modern integrated circuits (IC's) are metallized with aluminum. A compatible glass passivation process must therefore be performed under conditions where the maximum processing temperature is below the Al-Si eutectic temperature (577°C) to avoid alloying or metallization melting problems. Similar considerations hold for metallization systems involving gold. Chemical vapor deposition (CVD) of dielectric films at low temperature (300° to 500°C) is ideally suited to fulfill these requirements. Reactive sputtering, rf sputtering, and plasma deposition techniques can also be used for depositing dielectric layers, but their use is generally limited to certain applications and to devices that are not degraded by these treatments.

Glassing of microcircuit wafers was originally used to provide a mechanical protection against scratches of the soft aluminum interconnect lines. Vitreous silicon dioxide (SiO_2) prepared by CVD was first applied as the passivating glass, and is still being used by a number of IC manufacturers. However, to provide effective protection, an SiO_2 film thickness incompatible with the aluminum metallization is required, and cracking of the oxide film will generally result, with consequent problems of device reliability. Device manufacturers who have recognized these shortcomings have substituted more compatible lower-stress films of binary silicate glasses, especially phosphosilicate glass (PSG) films, for the more highly stressed SiO_2 layers.

Intrinsic stress in passivation films is a major factor in determining whether cracks occur in glass over metallization on IC's. Since cracks in the passivation glass can result in substantially lower IC reliability, a detailed knowledge of the effect of CVD deposition conditions on room-temperature stress of CVD films of SiO_2 and PSG on silicon wafer substrates would be of great value.

This paper presents a thorough survey of the subject matter and, in addition, provides new experimental data on the effects of systematic variations in deposition conditions on the film deposition rate, thickness uniformity, chemical composition, and intrinsic stress. The experimental results are examined in relation to data available in the literature. New results, therefore, are presented in the section to which they relate, rather than being grouped under a general discussion.

In addition, the effects of post-deposition storage and densification treatments on film stress are examined. Here, again, new experimental results are presented on the origin of localized structural defects in the glass layers. Analytical methods suitable for process control are also briefly outlined.

A large portion of this paper is contained in a report recently prepared by us on IC passivation by CVD techniques.[1] Several related papers should also be mentioned for reference: a summary of the effects of critical factors in the CVD of SiO_2 and PSG;[2] a survey of CVD reactor systems;[2,3] a discussion of functions, applications, and benefits of CVD passivation overcoatings;[3] studies on glass densification;[4] electrical properties of dielectric films;[5] new methods for defect detection;[6] and selective etching analysis of passivation films.[7,8] Finally, a comprehensive, recently published survey paper[9] reviews the entire field of silicon device passivation and may serve as a source of general background material in the present work.

2. General Considerations Pertaining to CVD Processing and Stress Measurements

2.1 Basic CVD Hydride Reactions

The basic process for depositing SiO_2 films from silane and oxygen at low temperatures (250° to 550°C) was reported in 1967.[10] The exact details of this thermally activated, surface-catalyzed, heterogeneous branching-chain reaction are complex.[11] The overall reaction can be expressed as

$$SiH_4(g) + 2O_2(g) \rightarrow SiO_2(s) + 2H_2O(g), \quad [1]$$

but under some circumstances it may proceed as

$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g). \quad [2]$$

The reaction favored depends strongly on deposition temperature and silane concentration,[10–14] and probably also on the oxygen-to-hydride ratio and variations in reactor geometry.

Phosphorus can be incorporated into the oxide layers as an oxide of phosphorus by the reaction of phosphine with oxygen,

$$2PH_3(g) + 4O_2(g) \rightarrow P_2O_5(s) + 3H_2O(g). \quad [3]$$

Co-oxidation with silane leads to phosphosilicate glasses.[14–19]

The preparation, properties, and applications of SiO_2 and PSG films synthesized from the hydrides and oxygen have been described extensively in the literature[10,12–32,68,69] and will be further referred to.

Specific effects of CVD parameters on the reaction chemistry are discussed in Section 4 of this paper.

2.2 Summary of Critical Factors in CVD

The exact conditions used in the CVD process for SiO_2 and PSG films can critically affect important film properties. Primary CVD parameters that affect deposited film properties, and must therefore be carefully optimized and controlled, include the following, listed in their approximate order of importance:

(1) Substrate temperature of deposition
(2) Oxygen-to-hydride ratio
(3) Hydride flow rate
(4) Silane-to-phosphine ratio
(5) Nitrogen flow rate
(6) Geometry of reaction chamber and gas inlet/outlet configurations
(7) Wall temperature of reaction chamber or gas disperser
(8) Impurities in CVD system and gases
(9) Gas additives
(10) Nature and cleanliness of substrate surface
(11) Geometry and topography of substrate
(12) Type of CVD reactor system

The effects of these factors on the film deposition rate, the thickness uniformity, the chemical composition (in the case of PSG), and the intrinsic stress are discussed and illustrated with experimental results in Sections 4 and 5.

2.3 Compatibility of Deposition Temperature with Metallization

The theoretical maximum temperature that can be used in processing devices metallized with aluminum is limited by the melting point of the eutectic formed between silicon and aluminum (577°C). In practice, however, the maximum temperature during glass deposition is held below 500°C because solid-state reactions between aluminum and silicon (or SiO_2) begin to exert degrading effects in many sensitive devices at approximately 500°C. Some reaction of aluminum with SiO_2 or PSG can be detected in certain devices at temperatures as low as 400°C, forming a thin intermediate layer of aluminosilicate, but normally this presents no serious problems if proper etching techniques are used in delineation of the glass layer to expose the bonding pads and scribe lines.

PSG overcoats have also been used over gold-metallized silicon devices.[33] In this application the temperature of glass deposition must

be kept below 350°C to avoid problems of eutectic formation between silicon and gold (373°C).

An up-to-date bibliography of many other related aspects of metallization materials for silicon devices became available recently.[34]

2.4 Layer Combinations

Combinations of PSG and SiO_2 layers can offer certain advantages over any one single layer. Structures consisting of SiO_2 over PSG, or of SiO_2/PSG/SiO_2, can be readily prepared by CVD techniques, often in one continuous operation, simply by regulating the hydride input in the gas stream.[17] A thin (1000-Å) CVD SiO_2 top layer over the phosphosilicate main layer of 0.6- to 1.5-μm thickness is desirable for improved photoresist adherence and consequently improved pattern etching definition, unless organo-silane adhesion-promoting agents are used. The composition of PSG layers used in the semiconductor industry is generally in the range of 2 to 5 wt % P (or 2 to 5 mol % P_2O_5).

2.5 Survey of Stress Measurement Methods

A variety of techniques for measuring stress in thin films are described in the literature.[1,35,36] X-ray and electron-diffraction analyses have been used to measure changes in lattice spacing and hence permit calculation of stress in films. However, more commonly, stress is calculated by optically measuring the deformation of a substrate, usually in the form of a beam, or a circular disc. In the beam-bending method, stress is calculated by determining the radius of curvature of the beam. Several methods for measuring the radius of curvature of a cantilevered beam have been reported.[35]

For a circular disc, the stress is calculated by measuring the displacement of the center of the circular disc in relationship to its edges. This can be accomplished by several methods: counting interference fringes between the disc and an optical flat, laser interferometry, holography, changes in location of the focal point, profiling the substrate with a light section microscope, or profiling the substrate by scanning with an optical microscope and measuring the change in focus from center to edge.[35,66]

2.6 Published Information on Stress in CVD Films

The literature contains some information on stress in CVD SiO_2 and PSG films.[1,9,26,37–42,66] Comparisons are sometimes difficult to make

because of the substantial differences in deposition systems and conditions. Generally, published data are based on room-temperature measurements. SiO_2 films have been reported to be in tension as deposited.[37] Because silicon has a higher coefficient of thermal expansion than silicon dioxide, the residual stress in low-temperature CVD SiO_2 films on silicon at room temperature is somewhat lower than the intrinsic stress of films as deposited, but the films are still in considerable tension.[37,42]

PSG films are in lower stress (at room temperature) than SiO_2 films deposited at the same conditions.[26,37] In general, however, residual stress at room temperature remains tensile.[26,41]

Some information is available on the effect of deposition rate[38,40] and silane/oxygen ratio[38] on CVD SiO_2 stress, and of phosphorus concentration on stress in CVD PSG.[26,40] Stress reduction in CVD films exposed to room air has been reported.[40,66]

Deposited SiO_2 or PSG films, when heated above the deposition temperature, are put in additional tension, particularly in regions over the edges of delineated aluminum films. Accordingly, there is some correlation between the intrinsic tensile stress in deposited films and the temperature increment above deposition temperature that can be attained before cracks begin to form.[26,37] In general, the lower the intrinsic stress in films, the thicker the CVD layer can be before severe cracking begins to occur.[18,26]

The relationship of device reliability and defects in deposited glass layers caused by intrinsic tensile stress and other properties of the glass/metallization system has been examined in recent papers.[1,9,26,43]

3. Experimental

3.1 Gases, Equipment, and Methods Used in CVD Studies

In most of the experiments reported here, semiconductor-grade 3.3 vol % SiH_4 and electronic-grade 1.0 vol % PH_3, both in ultrahigh-purity N_2, were used. Several premixed hydride compositions in nitrogen were also used in which the ratios of SiH_4:PH_3 were 6:1, 12:1, 23:1, and 60:1. The oxidant was O_2 of 99.9% purity, and the diluent was N_2 of 99.998% purity, both filtered through submicron filters.

Unless otherwise noted, we used a single-rotation vertical CVD reactor with a glass deposition chamber, described in a previous paper.[3] The hydrides with N_2 were introduced through the center inlet at the top of the chamber after having passed through a terminal submicron large-area filter. The O_2 was added to this gas stream before it entered the deposition chamber. Surface temperatures were measured

with bimetallic- and thermocouple-type surface thermometers. Other details on deposition technology were similar to those reported in previous papers.[3,17,19]

A variety of substrate materials were used for film deposition, but most of the work reported in this section was carried out with polished and chemically cleaned (100)-oriented single-crystal silicon slices of 5-cm diameter and 0.3-mm thickness.

Film thicknesses were measured by interferometric and profilometric techniques. The PSG composition was routinely analyzed by etch-rate measurements after densification of the films,[7] and by x-ray fluorescence methods; both techniques were calibrated by wet chemical analysis.

3.2 Methods Used for Stress Measurements

For the work described in this paper, the stress was determined by depositing films onto circular silicon wafers. Measurements of disc deflection were done at room temperature by three methods: (1) use of an optical flat and calculation of deflection by counting interference fringes;[44] (2) determination of the focal point by reflecting a collimated light off the surface of the wafer;[38] and (3) focusing an optical microscope on one wafer edge and moving the sample transversely from one edge to the other through the center of the wafer to measure the change in focus at various points. In this last method, measurements were made in both x- and y-directions at 5-mm intervals. The micrometer on the focusing dial was zeroed at the edge of the wafer. Upward and downward movement of the microscope stage was recorded as positive and negative, respectively. From this information, a plot of the wafer profile was constructed, from which deflection was determined.

Initially, all three methods were used to measure flatness of the substrate before CVD of the films. However, only method (3) was used in the latter part of the investigation, since it gave the best results. Corrections in the final graphical profile were made if deviations from flatness occurred in the starting substrate. Typical plots of change of focus versus distance across wafers are shown in the next Section.

Stress in the CVD films was calculated from the experimental data and the equation derived by Glang et al,[36]

$$\sigma = \left(\frac{\delta}{r^2}\right)\left(\frac{E}{3(1-\nu)}\right)\left(\frac{{t_s}^2}{t_f}\right), \qquad [4]$$

where

σ = stress (dynes/cm^2),
δ = deflection of disc (cm),
ν = Poisson's ratio for substrate,
E = Young's modulus of substrate,
t_f = film thickness (cm),
t_s = substrate thickness (cm), and
r = radius of disc (cm).

We also employed a convenient test based on step-wise heating of overcoat-passivated aluminum-metallized IC device wafers to relatively high temperatures (500° to 550°C) for typically 20 minutes per heating cycle to bring out latent stresses or weaknesses in the glass. These will increase in number with increasing temperature and give a realistic picture, suitable for statistical evaluation, of the potential stress levels and the specific location and distribution of excessive stress regions. This approach is akin to step-stress accelerated life-testing and constitutes a useful, practical test method, particularly in conjunction with aluminum marker-etching[45] to enhance the detection sensitivity of localized structural defects, especially microcracks, in the glass overcoating. The largest areas of undelineated aluminum within a circuit, such as those over large capacitors in linear bipolar IC's, are particularly sensitive to the onset of crack formation as a function of heat-treatment temperature. These areas are also most suitable for estimating the crack density, or for counting the number of cracks for quantitative statistical computations. This method of stress testing is by no means a substitute for the direct numerical measurement of film stress by the methods described above. It should be used in conjunction with them because it gives directly observable and realistic information not obtainable otherwise. The method is particularly useful for relative comparison of residual net stress in overcoat layer compositions and deposition conditions used for identical substrate IC wafers. Relatively small stress differences of overcoatings can be pictorially documented and compared by counting or estimating the density of microcracks for identical sample areas. Apart from overcoating parameters, the test is sample dependent; it is quite sensitive to the exact conditions of the substrate. The incidence of microcracks is a function of the thickness, area, and pattern geometry of the metallization, the taper angle and edge of the delineated metal lines, the prior annealing and alloying treatments, and the topography of the underlying oxide steps and via holes.

The use of unpatterned, planar aluminum films on oxidized planar silicon wafers for the test described above can provide additional

valuable information on the stress behavior of CVD films. Similar testing of the same films on polished silicon wafers as substrate is a further worthwhile variation of this test that we have used successfully.

4. Results and Discussion of CVD Studies

All of the critical factors in CVD of SiO_2 and PSG films listed in Section 2.2 have been investigated, and will be discussed in the order listed.

4.1 Effects of Temperature and Oxygen-to-Hydride Ratio

The effects of substrate temperature of deposition and O_2:hydride ratio are closely interrelated and are therefore best considered in the same context for both SiO_2 and PSG films. The effects on the deposition rate of SiO_2 and PSG are similar, and the composition of PSG is strongly dependent on both of these parameters.

We have previously shown[10] that SiH_4 diluted with N_2 begins to form SiO_2 films at a temperature of about 240°C if the O_2:SiH_4 mole ratio is in the range of 3:1. The rate of film growth at constant SiH_4 input increases rapidly as the substrate temperature is increased to 310°C. Further temperature increase to 450°C results in a very gradual increase in deposition rate. To attain a linear increase in the maximum deposition rate with temperature, the O_2:SiH_4 ratio must be increased as the temperature is increased. For example, at 475°C, an O_2:SiH_4 ratio of at least 14:1 is required to achieve this. Larger ratios of up to 33:1 have no effect, but ratios beyond this limit inhibit the reaction, leading to decreased rates of film growth. Thus, a plateau region exists at this temperature that is insensitive to the O_2:SiH_4 ratio. Temperatures lower than 475°C require progressively smaller O_2:SiH_4 ratios to attain the plateau of maximum SiO_2 deposition rate. At the same time the extent of the plateau region narrows as the temperature is decreased. These observations have since been confirmed by several other workers[13,14,22,31,32,46,68,69] and were found to hold qualitatively, even though different reactor geometries were used. The unusual reduction in SiO_2 deposition rate at high O_2:SiH_4 ratios has been explained by retardation theory where O_2 acts as the retardant by being adsorbed on the substrate surface.[14]

The corresponding observations for PSG formation by co-oxidation of $SiH_4 + PH_3$ with O_2 are essentially analogous to those discussed for SiO_2.[1,2,14,16,29] Fig. 1 shows plots of typical data we obtained studying the effect of O_2:hydride mole ratio on the deposition

rate of PSG at 350°, 400°, and 450°C. The SiH_4:PH_3 mole ratio was fixed at an intermediate value of 20:1, and the total gas flow rate was held constant at 11 liters per minute. The rate of PSG film deposition clearly depends on both the O_2:hydride ratio and the substrate temperature during deposition. The maximum deposition rate obtainable at a given temperature is a function of the O_2:hydride ratio. As the temperature is increased, the maximum deposition rate increases, but requires progressively larger O_2:hydride ratios to be attained. The semi-log plot in Fig. 1 indicates, furthermore, that the ratio range of the maximum region widens with increasing temperature.

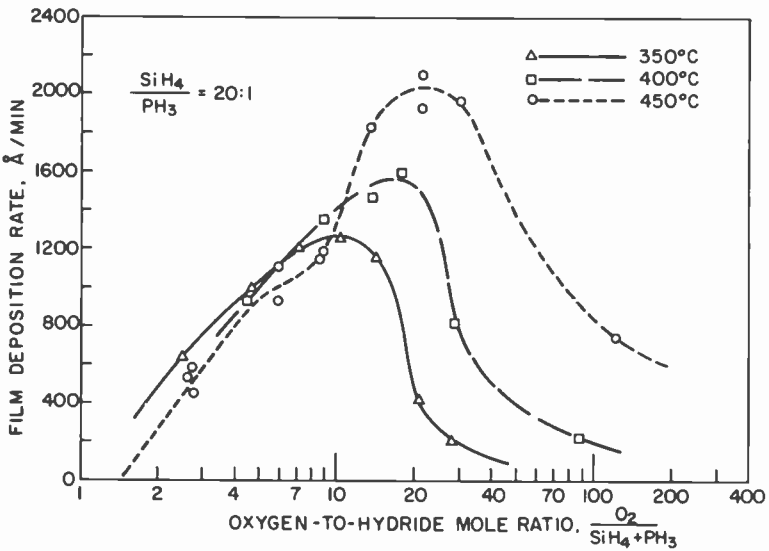


Fig. 1—PSG film deposition rate versus oxygen/hydride mole ratio for three deposition temperatures. Total gas flow rate was 11 liters/min.

Fig. 2 depicts the effects of O_2:hydride ratio and temperature on the composition of PSG films for the same samples and CVD conditions from which the deposition-rate results in Fig. 1 were obtained. The phosphorus concentrations in the glass films generally increase with both increasing O_2:hydride ratio and with decreasing temperature. The phosphorus content in the PSG films deposited at 450°C is less critically dependent on the ratio than in the films deposited at lower temperature, making the higher temperature considerably more desirable from a practical point of view, especially since the level-concentration range occurs within the O_2:hydride ratio range of

17 to 30, which also coincides with the range of maximum film deposition rate.

The effects of substrate deposition temperature for fixed O_2:hydride ratios are illustrated more directly in Figs. 3 and 4; they were both derived from Figs. 1 and 2.

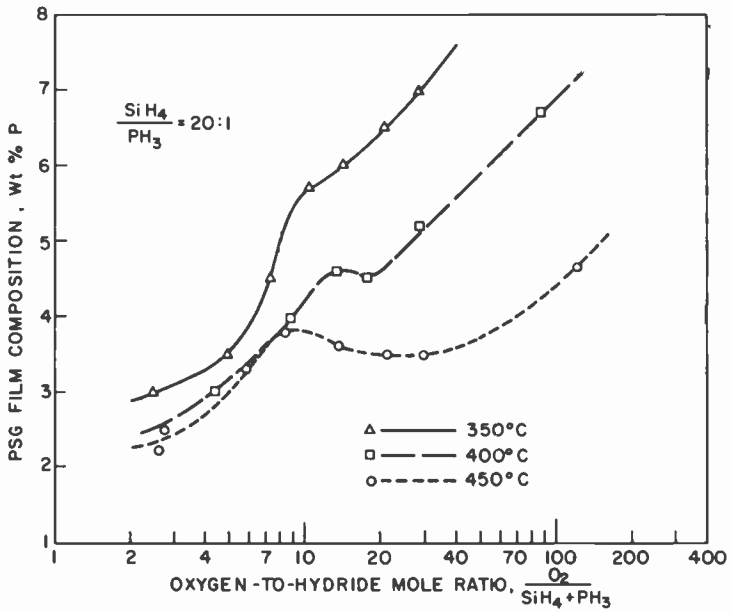


Fig. 2—PSG film composition versus oxygen/hydride mole ratio for three deposition temperatures. Total gas flow rate was 11 liters/min.

Fig. 3 shows the PSG film deposition rate at 350°, 400°, and 450°C as a function of selected O_2:hydride ratios (4:1, 6:1, 10:1, 24:1, and 30:1) and also for the ratios corresponding to the maximum deposition rate for each of the three temperatures. The curves exhibit negative slopes for the low ratios and change to positive slopes for the higher ratios. The curves indicate that the deposition rates at all three temperatures are similar for any one ratio in the lower range of 4:1 to 10:1 (not drawn for clarity) but differ increasingly as the ratio is increased. Again, the least dependence is noted at 450°C, where deposition rates at all high ratios (15:1, 24:1, and 30:1) are close to that at 22:1, corresponding to the maximum deposition rate.

Fig. 4 shows the PSG phosphorus concentration as a function of the same O_2:hydride ratio values selected for Fig. 3, again for all three

temperatures. Also included in this figure is a plot showing the temperature effect for a lower SiH_4:PH_3 mole ratio (7.7:1) over an extended temperature interval (310° to 450°C); the O_2:hydride ratio was held constant at 24:1. The difference between the slope of this curve and the 24:1 curve for the higher SiH_4:PH_3 ratio (20:1) indicates some dependence of the temperature effect on the hydride ratio. The family of curves for the 20:1 SiH_4:PH_3 ratio series shows

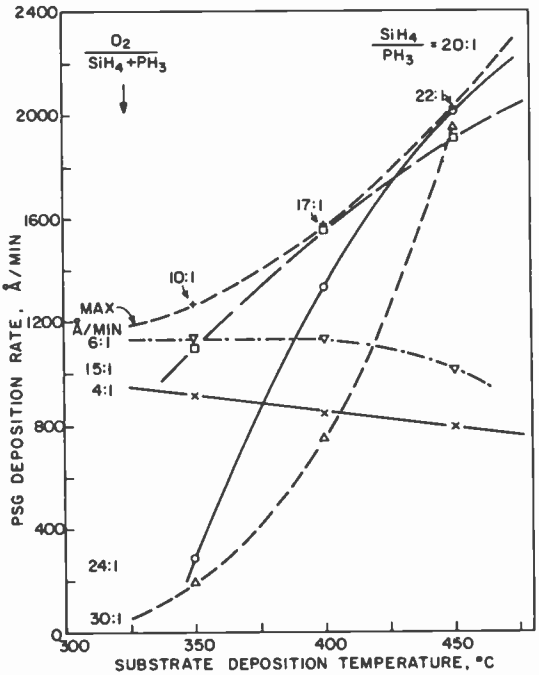


Fig. 3—PSG film deposition rate versus deposition temperature for selected oxygen/hydride mole ratios at a SiH_4/PH_3 mole ratio of 20:1. The top curve, marked Max Å/min, corresponds to ratios yielding maximum deposition rates. All values were taken from Fig. 1.

that the effect of temperature on PSG composition becomes progressively less as the O_2:hydride ratio is decreased, similar to the effect on deposition rate. Again, the curves for the higher ratios converge at 450°C, demonstrating minimum dependence. The curve corresponding to the O_2:hydride mole ratios of maximum deposition rate is a straight line.

An immediate practical consequence of the temperature effect is the need for isothermal surface conditions of the substrate wafer. Good thermal contact of the wafer with the heated substrate plate is essential to effect good heat transfer and to avoid thermal variations in the wafer surface. Poor contact may arise if the wafers are warped (possibly due to improper annealing after diffusion), if wafers overlap on positioning, or if excessive quantities of CVD glass are allowed to accumulate on the substrate plate causing a decrease in the surface temperature.

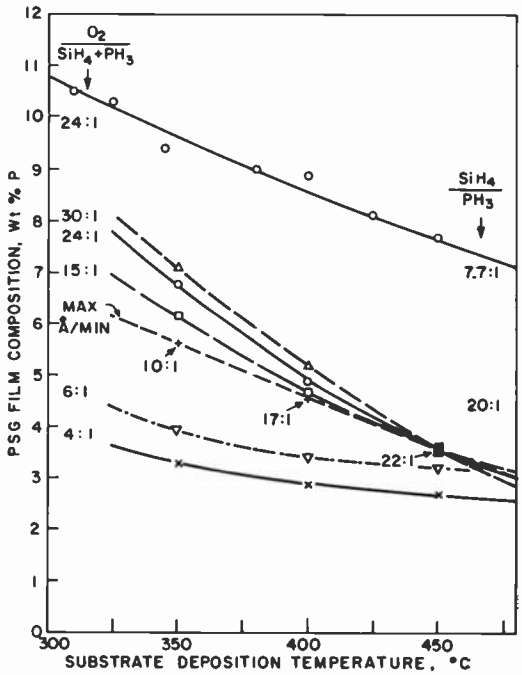


Fig. 4—PSG film composition versus deposition temperature for selected oxygen/hydride mole ratios. The family of lower curves was plotted from values taken from Fig. 2. The curve marked Max. Å/min corresponds to ratios yielding maximum deposition rates. The top curve shows temperature effect on composition for a silane/phosphine ratio of 7.7:1 at constant oxygen/hydride ratio of 24:1.

The results we have presented here agree very well with data reported in the literature cited in this section, even though different CVD reactor systems and conditions were used.

4.2 Effects of Hydride Flow Rate

The quantity of SiH_4 or of $SiH_4 + PH_3$ introduced into the reaction chamber per unit time at a constant substrate temperature and O_2:hydride ratio determines the rate of film deposition, which follows a linear function up to some saturation level limited by the size and geometry of the reaction chamber. In other words, the film thickness increases proportionally with the hydride input and the time period of deposition, independent of the film thickness up to many micrometers, at which point decreased thermal conductance may become noticeable. Hydride input quantities for the reactor system we used to obtain the data in Figs. 1 and 2, for example, were 670 cm^3/min of 3.3% SiH_4 and 110 cm^3/min of 1.0% PH_3. The PSG film composition is affected only slightly by very large variations in the film-deposition rate, so that this effect can be disregarded in practical applications.

4.3 Effects of Silane-to-Phosphine Ratio

The SiH_4:PH_3 ratio under otherwise constant CVD conditions determines the composition of the resulting PSG. The relationship of the mole ratio of SiH_4:PH_3 in the gas and of SiO_2:P_2O_5 in the resulting glass is nearly linear,[1,2,26,29] as shown in Fig. 5, for a deposition temperature of 445°C. A plot of the same data in terms of mol % PH_3 in $SiH_4 + PH_3$ versus mol % P_2O_5 in $SiO_2 - P_2O_5$ in the resulting PSG is presented in Fig. 6. It shows a linear relationship up to about 10 mol % P_2O_5, followed by a less than linear increase in P_2O_5 beyond this point. Recent data reported in the literature[29] agree within approximately 10% with our curve shown in Fig. 6. Lower temperatures of deposition at constant SiH_4:PH_3 ratio increase the mol % P_2O_5 in the PSG if the O_2:hydride ratio is adjusted for the plateau region of maximum deposition rate for each temperature, in agreement with the data shown in Fig. 4 and with literature data.[29]

The relationship depicted in Figs. 5 and 6 indicates that the PSG resulting from the oxidation under the conditions stated contains more phosphorus than would be expected from stoichiometry, since two moles of PH_3 form one mole of P_2O_5. Fig. 6 indicates that up to about 10 mol % P_2O_5 the conversion efficiency of PH_3 to P_2O_5 at 445°C is 1.4 times greater than that of SiH_4 to SiO_2. At lower temperatures it is still greater. Stated differently, the conversion efficiency of SiH_4 to SiO_2 during co-oxidation of $SiH_4 + PH_3$ is lower than that of PH_3 alone. Apart from kinetic[14] and thermodynamic[27] differences in the oxidation of the two hydrides, the previously mentioned retardation of SiH_4 oxidation by oxygen is almost certainly responsible for

at least part of the observed effect. Hence, higher than expected phosphorus concentrations in the PSG result. In addition, PH_3 appears to have a retarding effect on SiH_4 oxidation, since our work as well as literature data[30,32] indicates that the film deposition rate is depressed by small additions of PH_3. We have obtained similar results of retardation with diborane in the co-oxidation of $SiH_4 + B_2H_6$ to deposit borosilicates.

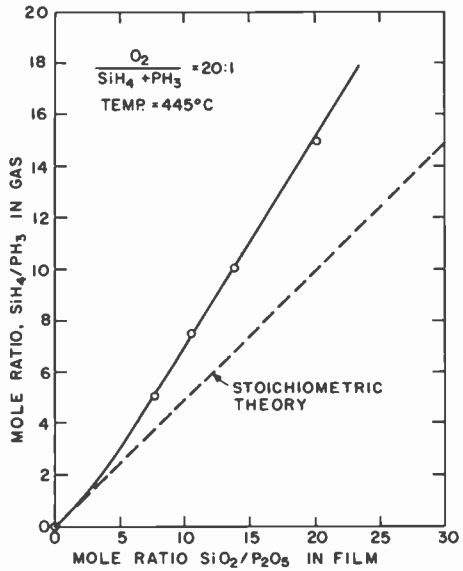


Fig. 5—Mole ratio SiO_2/P_2O_5 in PSG film versus mole ratio SiH_4/PH_3 of the hydride gas mixture at a substrate deposition temperature of 445°C and an oxygen/hydride ratio of 20:1. The dashed line indicates relationship for stoichiometric reaction. Total gas flow rate was 8 liters/min. Film deposition rate was 4000 Å/min. Film analysis based on wet chemical method.

Incorrect SiH_4:PH_3 ratios can lead to several problems in the glass. A PSG with low phosphorus content may result in inadequate gettering of externally introduced contaminants such as sodium ions; it may also cause cracking of the glass because of excessive stress. Too high a concentration of phosphorus, on the other hand, may result in current leakage across the surface or in a hygroscopic glass, which may cause metal corrosion problems.

In adjusting the hydride ratio for otherwise fixed conditions, it is convenient to use a plot of etch rate values of the films as a direct function of the SiH_4:PH_3 ratio.[1,7]

4.4 Effects of Nitrogen Flow Rate

The function of the diluent nitrogen is threefold: (1) to dilute the reactive gases to a sufficiently low concentration to prevent spontaneous combustion when combined with the oxygen and, in some systems, to afford premixing; (2) to force the reactive gas mixture over the heated substrate surface; and (3) to create gas-flow conditions in the reaction chamber that result in good film uniformity across a maximum area of the substrate plate. Too low a nitrogen flow rate

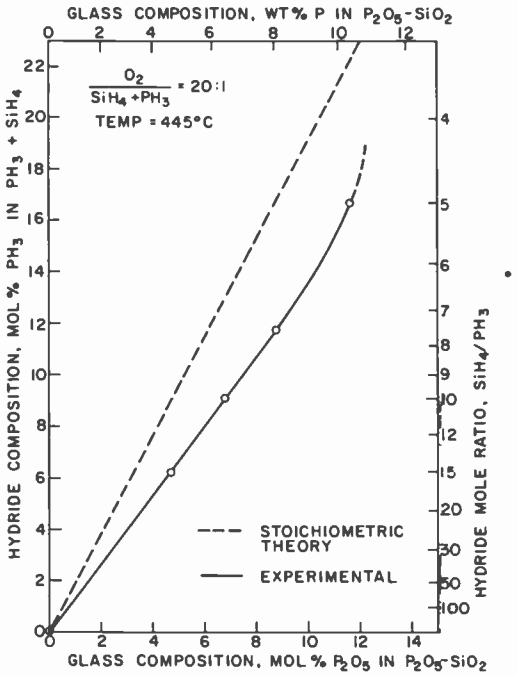


Fig. 6—Composition of PSG films versus composition of hydride gas mixture. Samples and CVD conditions are the same as those defined in Fig. 5. Also shown are PSG composition in terms of wt % P and hydride composition in terms of mole ratio.

can severely depress the deposition rate of both SiO_2 and PSG films and lead to gross nonuniformities in film thickness across the wafers. Excessive nitrogen flow decreases the residence time for the gases at the substrate surface and causes the plate temperature to drop due to

cooling, thus leading to nonuniform deposits that, in the case of PSG, contain more phosphorus than obtained under normal conditions (because of the decreased temperature as indicated in Figs. 3 and 4). A suitable flow rate for our reaction chamber (described in Refs. [1] and [3]) is in the range of 7 to 11 liters of total N_2 (including hydride diluent N_2) per minute, the correct quantity being determined by the attainment of good film-thickness uniformity under the specific CVD conditions used.

Silane, despite its reactivity at high concentrations with oxygen, can be conveniently premixed for production applications with oxygen and nitrogen at sufficiently high dilutions in both oxygen and nitrogen (i.e., 0.5% SiH_4, 2.5% O_2, 97% N_2 by volume), forming a mixture that is inert until heated above 200°C.[13,27]

4.5 Effects of Reactor Geometry

The shape and dimensions of the reaction chamber and the gas inlet/outlet configuration are very critical with respect to thickness uniformity of the film deposits because they affect the flow dynamics of the gas stream. We have constructed and tested many reaction chambers and found that small differences can cause gross effects, particularly in single-rotation reactors, where a lesser degree of averaging is attainable than in planetary units. The type of bell jar described in Refs. [1] and [3] has given particularly good results despite its deceptive simplicity.

4.6 Effects of Reaction Chamber Wall Temperature

The reactor wall, if hot, acts as a substrate for both glassy and powdery gas-phase reaction products. Cooling the reactor parts that are not intended for heating the substrate results in a decrease of these undesirable coatings and also suppresses homogeneous gas phase nucleation, which is the cause of the powdery deposits, while at the same time promoting desirable heterogeneous reactions leading to glassy films. As a consequence, cleaner film deposits form and the deposition rate tends to increase for the same reactant input. This means, in effect, that the yield of glassy product can increase considerably, since the input of expensive reactants can be reduced to attain the same deposition rate obtained with a hot-wall reactor. The composition, in the case of PSG films, can be slightly affected by this change, requiring some readjustment of the SiH_4:PH_3 ratio.

4.7 Effects of Impurities in CVD System and Gases

The surface-catalyzed free-radical reaction mechanism underlying CVD of oxide and glass films is quite sensitive to particulate contaminants in the gas phase. Particles in the gas stream (mainly colloidal oxides formed by premature reaction) can cause microbubbles, pinholes, and other localized structural defects in the glass layer. A number of authors have pointed out the relationship between pinholes in dielectric films and particulate impurities in CVD systems and gases.[1,2,3,9,45,46,69] It is therefore imperative to suppress the formation of particulate impurities effectively and to remove as much as possible of the impurities that still form by use of large-area high-capacity submicron filters in the gas lines positioned as close to the site of film deposition as practicable. Frequent blasting out of the CVD system and the gas lines with pressurized nitrogen to dislodge and remove particles is very convenient and effective. In addition, periodic cleaning of the CVD reactor and the gas tubing system should be carried out.

Another type of impurity in CVD films arises from chemical contaminants in the gases used. Silicon dioxide films deposited from semiconductor-grade silane and oxygen are known to contain some sodium that may deleteriously affect MOS devices.[1,26] In the present work, atomic absorption analysis was used to assess the concentration of alkali impurities and copper in typical SiO_2 and PSG films of 1 to 2 μm thickness that were prepared at 300° and 450°C in the rotary CVD reactor at deposition rates ranging from 300 to 2000 Å/min. The impurity contents in parts per million by weight ranged as follows: Na 2–6, K 1–3, and Cu 0.6–1.4. Fortunately, PSG passivation layers of proper composition are capable of gettering alkali contaminants to the extent that device instability problems due to this cause should not arise with typical device structures.

4.8 Effects of Gas Additives

Additives to the CVD reaction were investigated for the purpose of either lowering intrinsic stress in the glass films or for suppressing homogeneous gas phase nucleation.

Stress in SiO_2 and PSG was successfully lowered by adding water vapor to the gas stream entering the deposition chamber. Quantitative details of these experiments are discussed in Sections 5.7 and 5.8. We found that the deposition rate of SiO_2 films is not markedly affected by the addition of water vapor, in agreement with previously reported observations.[1,31,68] We also found that neither the deposi-

tion rate nor the composition and uniformity of PSG films is noticeably influenced by introducing water vapor during CVD. Additions of azeotropic hydrochloric acid (20% HCl) vapor instead of water vapor for the purpose of possible impurity gettering also did not affect deposition rate, uniformity, composition of PSG films, or the aluminum metallization of IC wafers being glass coated.

As already noted, most of the particular contaminants present in CVD systems are caused by homogeneous gas phase nucleation (manifested as white fog and powdery wall deposits) that can be minimized to some extent by the techniques noted. Complete but selective suppression of the homogeneous reaction by addition of a specific inhibiting agent (such as a free-radical scavenger) to the gas mixture during CVD would be highly desirable to improve the quality of the glass layers. Ethylene has been reported to act as a selective suppressant of homogeneous gas phase nucleation in the oxidation of silane to SiO_2;[31] however, selective inhibition is effective only at very low O_2:SiH_4 ratios[47] (such as 1.5:1) where formation of colloidal oxide is extreme.[10] Because of the decreased rates of film growth, these conditions are not normally usable for film deposition. Experiments conducted in our laboratory using a rotary reactor, O_2:SiH_4 ratios of 6:1 and 15:1, deposition temperatures of 350° and 450°C, total gas flow rate of 11 liters/min, and ethylene additions yielding C_2H_4:SiH_4 ratios ranging from 0.3:1 to 100:1 showed the following. Ratios of C_2H_4:SiH_4 of less than 1:1 did not markedly affect the deposition rates of either the vitreous SiO_2 (1100 Å/min) on the silicon substrates or that of the powder on the reactor wall. Higher ratios caused a rapid, but nonselective depression of the deposition rates for both products. For example, a ratio of 5:1 led to a 11-fold decrease in the film deposition rate. Ratios of 14:1 to 100:1 completely prevented any reaction.

Results obtained with PSG at a substrate temperature of 450°C and at O_2:hydride ratios of 8:1 and 20:1 showed that the film deposition rate is also suppressed nonselectively, but more severely than in the case of SiO_2. A C_2H_4:hydride ratio of only 5:1 completely inhibited reaction.

Similar results of nonselective inhibition of SiO_2 and PSG formation were also obtained with styrene and several other selected compounds.

4.9 Effects of Substrate Surface

The composition of the substrate material and the physical and chemical nature of adsorbed contaminants on the substrate surface affect the growth rate and the quality of CVD oxide and glass films

Table I—Effects of Substrate Impurities on the Microscopic Appearance of CVD SiO_2 and PSG Films (Defects Observed by White Light, Monochromatic Light, or Nomarski Differential Interference Contrast)

Contaminant Added to Substrate	Polished Si Substrate Wafer		Evaporated Al Film on SiO_2	
	SiO_2	PSG	SiO_2	PSG
Control				
No contaminants added	(H)	No defects	(H)	(H)
Particulates				
Si crystal dust	H	H	E,H,P	E,H
Al_2O_3 powder, 0.05 μm particles	H (Fig. 7E)	H	E,H,P	E,H,K
PSG dust, CVD wall deposit	H (Fig. 7A)	B,E,H	E,H	E,H
Organics				
Apiezon	C,H,K,T	B,S	B,D (Fig. 7B)	B
Photoresist	D,S	(H),(S)	H,K,P	C
Trichloroethylene	C,H,S,T	D,H,K,S	H	E,H
Chemicals				
HF, poorly H_2O rinsed	H,K,S,T	P	C,H	C
HF + HNO_3, poorly H_2O rinsed	H,S	H	H	E,P,K
H_3PO_4, poorly H_2O rinsed	C,S	D,K,P,S (Fig. 7F)	H,P	P
Mixed				
Tap water	D,S,Y (Fig. 7C)	S,Y	H,P	H,P
Fingerprints	Y (Fig. 7D)	Y	Y	Y

Code of Defects:
B - Bubbles or blisters
C - Cloudy, hazy
D - Dots or micropinholes
E - Elongated interference fringe patterns
H - Halos of interference fringes
K - Streaks
P - Pits or depressions
S - Stains
T - Thin spot areas
Y - Crystals

( ) indicates small number of defects only.

synthesized from the hydrides.[1–3,10,15,17,19,22,67,70] This is in part due to the free-radical reaction mechanism underlying this type of hydride oxidization, which is sensitive to chemical trace impurities on the substrate surface that can act as growth catalysts or inhibitors.

Effects of usually nondescript substrate impurities on CVD SiO_2 films have been reported by several investigators.[1,10,22,43,45,46,48] In general, defects such as pinholes, pits, thin spots, blisters, microbubbles, cloudiness, and local variations in film thickness can result. To examine under controlled conditions the effects of specific substrate impurities on the microscopic appearance of CVD SiO_2 and PSG films, selected representative physical and chemical materials were placed randomly on certain areas of clean substrates, which were then overcoated under typical CVD conditions at 450°C. The substrates consisted of polished and chemically cleaned (100)-oriented silicon wafers and of 5000 Å-thick unpatterned aluminum films vacuum evaporated over thermally oxidized polished silicon wafers. Samples without additives served as uncontaminated controls. Particulate impurities, sprinkled over the substrates, were silicon crystal dust from scribing with a diamond, aluminum oxide powder (γ-Al_2O_3, cubic) of 0.05-μm-diameter particles, and PSG power from CVD reactor wall deposit. Organic contaminants, applied to the substrate from solution and allowed to dry, included Apiezon Hard Wax W (J. G. Biddle Co.), KTFR photoresist (Eastman Kodak Co.), and electronic grade trichloroethylene. Reactive chemical agents were oxide etch (49% HF solution), silicon etch (49% HF–70% HNO_3 1:1 mixture), and aluminum etch (85% H_3PO_4-H_2O–70% HNO_3 40:10:4 mixture). In this series the substrates were immersed in the reagents and rinsed briefly with a small amount of distilled water. Additional sample impurities were tap water allowed to dry on the substrates and fingerprints leaving NaCl and greasy impurities. The results of microscopic examination of the samples after CVD are summarized in Table 1. Photomicrographs of several typical defects observed are presented in Fig. 7.

4.10 Effects of Geometry and Topography of Substrate

The relief geometry of the structure and the topography of the substrate surface determine to a significant extent the quality of the CVD glass overcoat, apparently due to localized disturbances in the gas flow pattern.

The layer integrity and conformity over steep steps and sharp edges are particularly severely affected by these factors, and can give rise to serious reliability problems, as is evident by analysis of glass-

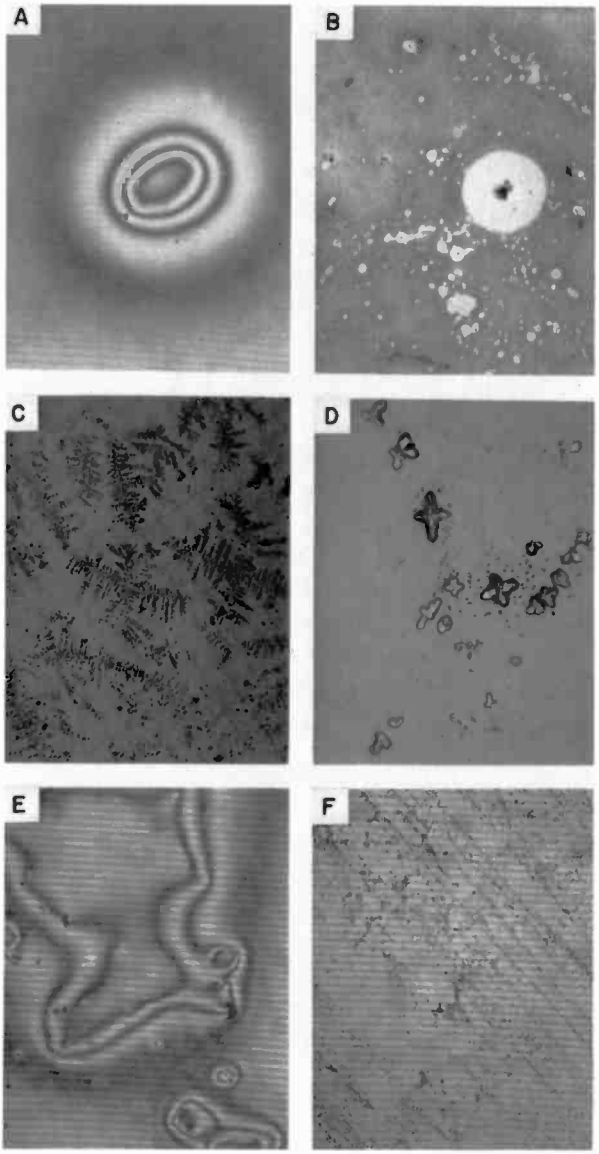


Fig. 7—Photomicrographs showing typical effects of surface contaminants on the microscopic appearance of CVD overcoatings defined in Table 1. Magnifications are for photo sizes shown here:

A–SiO_2 over PSG particles on Si (monochromatic light, X93)

B–SiO_2 over wax residue on Al (white light, X180)

C–SiO_2 over tap water residue on Si (Nomarski differential interference contrast, X230)

D–SiO_2 over NaCl crystals from fingerprints on Si (white light, X180)

E–SiO_2 over γ-Al_2O_3 particles on Si (monochromatic light, X93)

F–PSG over H_3PO_4 residue on Si (monochromatic light, X230)

passivation device failure modes.[1,43,45,49,50] We have previously shown[49] that the quality of step coverage can be controlled and improved to a limited extent by optimizing the CVD conditions (mainly by reducing the total gas flow rate), although tapering of the structure prior to overcoating should be done whenever possible because it is more effective.

New results indicate that the chemical composition of an overcoating material can have a marked influence on the step coverage. Layers of 0, 2, 3, and 4 wt % phosphorus PSG of 1.1 to 1.2-μm thickness were deposited on wafers of two types of aluminum-metallized IC's (planar linear bipolar and MOS IC's). Deposition was carried out at 450°C in a rotary reactor at a rate of 2000 Å/min. We found, by special etching techniques,[6] that 2 to 4 wt % phosphorus PSG affords a substantially better conformal edge coverage over aluminum patterns than does SiO_2 (0% P). The difference between 0 and 2 wt % phosphorus is remarkable, and is definitely due to the overcoat material since the conditions of CVD were kept exactly analogous, and the effect occurred on both types of IC's, even though the aluminum thickness and edge contour are not exactly the same.

Surface roughness of the substrate is another factor that determines the quality of CVD layer deposits. A typical case is that of evaporated aluminum films, especially after alloying treatments with silicon, which leads to the formation of hillocks, spikes, and grainyness that tend to give rise to increased pinhole formation in the overcoating.[1,48]

4.11 Effects of CVD Reactor Systems

A considerable variety of CVD reactor systems for preparing SiO_2 and PSG passivating overcoatings is now available. We have categorized and described the design, operation, and capability of CVD equipment, which varies from relatively simple to sophisticated automated reactors.[1–3] We have conducted a limited number of experiments with several of these types of reactor systems, including several commercially available continuous processing units,* to examine whether the experimental results presented in this section are applicable to other systems as well. We found that they not only agree in principle, but that they frequently relate on a semiquantitative basis, despite the remarkable differences in geometry and system operation.

* Typical units and their manufacturers are as follows: Rotox-60, Unicorp. Incorporated, 625 North Pastoria Dr., Sunnyvale, CA 94086; AMS-2000 Continuous Silox Reactor, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA 95051; PWS Model 2000 Vapor Deposition System, Pacific Western Systems, Inc., 855 Maude Avenue, Mountain View, CA 94040.

Nevertheless, the performance of each reactor must be carefully examined and adjusted to attain conditions for producing films of specified properties.

5. Studies of Film Stress

5.1 Evaluation of Substrates Used for Stress Measurements

Initially, 65-μm-thick, flat, circular (111)-oriented silicon wafers were used as a substrate to measure the stress of deposited films. During the CVD process the wafers deformed because of the thermal gradients across them, as well as from the strain that was being introduced from the depositing layer. (The magnitude of the deformation of these thin silicon test wafers is, of course, much greater than that which occurs on the considerably thicker integrated-circuit wafers.) Deformation of the substrate during CVD can cause errors in the stress measurements; it is therefore important that the substrates remain relatively flat during film deposition. To maintain the flatness, a fixture was designed to hold the substrates down by vacuum. The fixture consisted of an aluminum block 57 mm in diameter and 18 mm in height, with a 6.3-mm stainless-steel tube leading to a cavity in the center of the block; 0.3-mm holes were drilled through the top of the block to the cavity, in a circular area 35 mm in diameter. A vacuum line was connected to the fixture, and wafers placed over the holes in the top surface were held firmly in place.

While the vacuum hold-down fixture worked satisfactorily, it could not be used with some types of CVD reactors. Furthermore, the 65-μm wafers proved to be too fragile for easy handling in a large number of tests. Accordingly, tests were carried out to determine what wafer thickness could be used that would not be excessively fragile and still give good results. It was found that wafers about 140 μm thick and 39 mm in diameter were sturdy enough so that excessive breakage did not occur. Because of the increased thickness, it became unnecessary to use the vacuum hold-down fixture. Stress measured on samples held fast during deposition was not appreciably different from that of wafers not held at all, and uniform CVD film thicknesses resulted. Profiles for two wafers, one with and one without hold-down, are shown in Fig. 8.

The term $E/(1 - \nu)$ in the stress equation (Eq. [4]) was calculated for the silicon substrates used for film deposition. This was accomplished by thermally oxidizing the wafers in steam at 1100°C, removing the oxide from one side in aqueous HF, and measuring the deflection. Since the stress value of thermally grown SiO_2 has been pub-

lished,[51] this value was substituted into the stress equation, and $E/(1 - \nu)$ was calculated. The calculated value of 1.9×10^{12} dynes/cm^2 for (111)-oriented silicon is close to Glang's value of 2.3×10^{12} dynes/cm^2.

However, for (100)-oriented silicon, the value of $E/(1 - \nu)$ was found to be 1.3×10^{12} dynes/cm^2. This difference between (111) and (100) silicon was also confirmed by stress experiments, which showed that wafers of equal thickness with equal CVD oxide thicknesses deflected by different amounts, with larger deflection occurring on (100)-oriented silicon wafers.

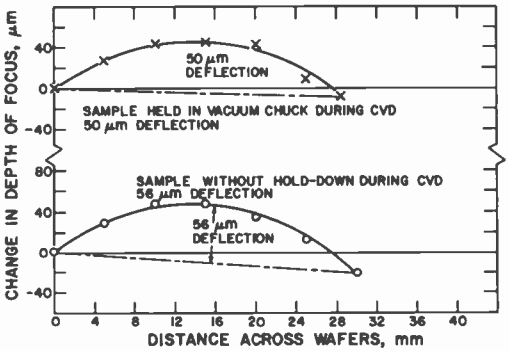


Fig. 8—Profiles of two silicon substrates following CVD of a 1-μm-thick layer of SiO_2.

In the process of making stress measurements in CVD dielectric layers, some unexplained variations in measured stress were observed. Experiments revealed that some substrate wafers deflected more easily than others, thus indicating larger stress value than actually were present in the CVD layer. Variations in the depth of microcracks caused by lapping and polishing of the silicon substrate are probably the main cause for the difference between wafers. In an effort to eliminate these variations, an apparatus was set up to measure wafer deflection by placing the silicon substrates onto an O-ring support, and then applying a partial vacuum to the holder, thus causing the wafer to bow. A differential pressure of 14.7 Torr was used, since this deflected the substrates about the same amount as a CVD SiO_2 film of 1 μm thickness. Each wafer used for stress measurements was checked, and only wafers that showed equal amounts of deflection for both sides and equal amounts of deflection from wafer to wafer for a given pressure were used for stress measurements of deposited films.

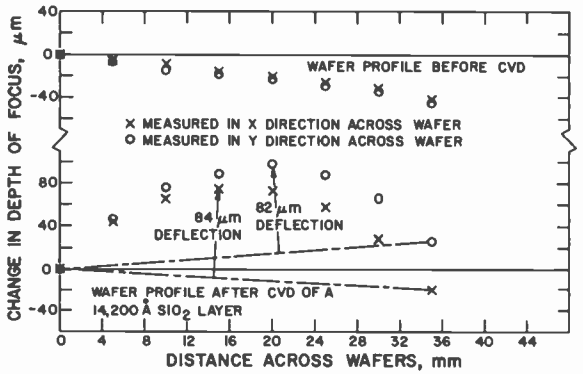


Fig. 9—Wafer profiles before and after CVD of a 1.4-μm-thick SiO_2 layer.

For all stress data presented in this report, (111)-oriented silicon substrate wafers were used, and Glang's value[36] for $E/(1 - \nu)$ was used in the calculations. Typical plots of change of focus versus distance across a wafer before and after coating are shown in Fig. 9 to illustrate the measurement method.

5.2 Effect of Storage on Stress

Stress in CVD SiO_2 films decreases with time, the amount of decrease being dependent upon the storage ambient. Wafers having a CVD SiO_2 layer are essentially relieved of their stress in about four hours if stored in 100% relative humidity at room temperature, whereas films prepared under the same deposition conditions showed little change in stress when stored in a dry box for 70 hours (Fig. 10). Wafers with oxide layers whose stress had been relieved by storing in 100% rela-

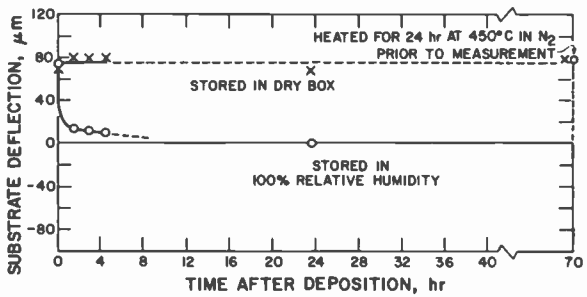


Fig. 10—Plot of wafer deflection as a function of storage ambient and time.

tive humidity went back into tensile stress when the sample was returned to the dry ambient. These results indicate that for undensified, encapsulated SiO_2 layers, the stress will vary depending on ambient conditions.

5.3 Effect of Deposition Rate on Stress

SiO_2 films deposited at 350°C at a deposition rate of 400 Å/min had a tensile stress of 2.5×10^9 dynes/cm^2. At a deposition rate of 1400 Å/min the stress increased to about 3.1×10^9 dynes/cm^2. Measurements of SiO_2 films deposited at 450°C and at a very high rate (5000 Å/min) showed a tensile stress of about 3.4×10^9 dynes/cm^2, as compared with 2.7×10^9 dynes/cm^2 for films deposited at 1000 Å/min.

Stress as a function of film deposition rate for PSG layers deposited at 400°C and containing 3.6 wt % phosphorus was measured in the range of 1250 to 5000 Å/min with the O_2:hydride ratio held constant at 11.4:1. Stress was 2.3×10^9 to 2.4×10^9 dynes/cm^2 for all samples prepared in this range.

5.4 Effect of Deposition Temperature on Stress

Stress as a function of deposition temperature was measured in the range of 340° to 450°C. The average stress for five samples of CVD SiO_2 films on silicon prepared at 340°C was 3.1×10^9 dynes/cm^2. Film average stress for five samples prepared at 400°C was also 3.1×10^9 dynes/cm^2. Samples prepared at 450°C averaged 2.7×10^9 dynes/cm^2. The etch rate tends to decrease with increasing deposition temperature. Experimental conditions and evaluation data for these and similar tests are presented in Table 2.

5.5 Stress as a Function of Oxygen-to-Hydride Ratio

Stress as a function of O_2:SiH_4 ratio was measured for SiO_2 films deposited at 450°C, and little difference was observed in the stress of the deposited film when the O_2:SiH_4 ratio was varied between 3:1 and 36:1, as shown in Table 3. Low O_2:SiH_4 ratios have been reported[38] to produce lower stress CVD SiO_2 films at 400°C.

We have found that the stress in CVD PSG overcoatings can be strongly influenced by the O_2:hydride ratio. In these experiments the deposition temperature was lowered to typically 400°C with deposition rates of approximately 2500 Å/min. PSG films of 15,000 to 19,000 Å thickness and containing 9–12 mol % P_2O_5 were deposited over IC wafers. Induced stress crack testing at 530°C showed no

Table 2—Relationship of Stress in CVD SiO_2 Films and Deposition Temperature (N_2 diluent flow rate: 6000 cm^3/min; O_2 flow rate: 687 cm^3/min; deposition time: 10 min)

Sample No.*	Film Thickness (Å)	Deposition Rate (Å/min)	Etch Rate† (Å/sec)	Stress (dynes/cm^2)
Deposited at 340°C; 10% SiH_4 in Ar at a Flow Rate of 375 cm^3/min				
1	10,970	1,100	—	2.7×10^9
2	11,200	1,120	17.8	3.1×10^9
3	14,000	1,400	—	3.2×10^9
4	11,570	1,160	17.2	3.2×10^9
5	9,540	950	18.9	3.4×10^9
Deposited at 400°C; 10% SiH_4 in Ar at a Flow Rate of 325 cm^3/min				
6	12,620	1,260	17.0	3.6×10^9
7	17,600	1,760	16.6	2.9×10^9
8	13,800	1,380	—	3.3×10^9
9	14,100	1,410	17.5	3.0×10^9
10	12,380	1,240	—	3.3×10^9
Deposited at 450°C; 10% SiH_4 in Ar at a Flow Rate of 233 cm^3/min				
11	11,140	1,110	—	2.8×10^9
12	10,730	1,070	—	2.7×10^9
13	12,700	1,270	16.6	2.6×10^9
14	12,570	1,260	16.3	2.8×10^9

*Samples were prepared on different dates.
†P-etch at 25.0°C.

cracks in films deposited with O_2:hydride ratios of 10:1 and lower, some cracks at a ratio of 20:1, and a very high density of cracks at a ratio of 40:1.

5.6 Stress as a Function of Glass Composition

A number of investigators[1,9,18,26,50,52] have reported lower stress for PSG layers compared to SiO_2, and that the stress tends to decrease as

Table 3—Relationship of Stress in CVD SiO_2 Films and O_2/SiH_4 Ratio (Deposition temperature: 450°C; N_2 flow rate: 6 liters/min; 10% SiH_4 in Ar at a flow rate of 190 cm^3/min)

O_2:SiH_4 (Ratio)	O_2 Flow Rate (cm^3/min)	Oxide Thickness (Å)	Deposition Rate (Å/min)	Tensile Stress (dynes/cm^2)
36:1	687	12,600	1,260	2.9×10^9
14:1	263	14,200	1,420	2.8×10^9
3:1	60	11,900	1,190	3.2×10^9

the phosphorus concentration in the glass is increased. In agreement with this, our experiments have shown that as the phosphorus content in a CVD PSG layer increases from 0 to 8.5 wt %, the room temperature stress decreases. Stress for pure SiO_2 films deposited at 450°C at 10,000 Å/min averages 3.1×10^9 dynes/cm^2, for the PWS 2000 continuous reactor. As one increases the phosphorus content to 8.5 wt % and maintains the film deposition rate at 10,000 Å/min (450°C), the tensile stress at room temperature is reduced to essentially zero. However, upon densification at 1000°C, the layer went into a compressive stress of 1.3×10^9 dynes/cm^2. Results thus show that room-temperature stress in CVD films can be reduced to nearly zero by increasing the phosphorus content; however, excessively high concentrations of phosphorus can lead to electrochemical attack of

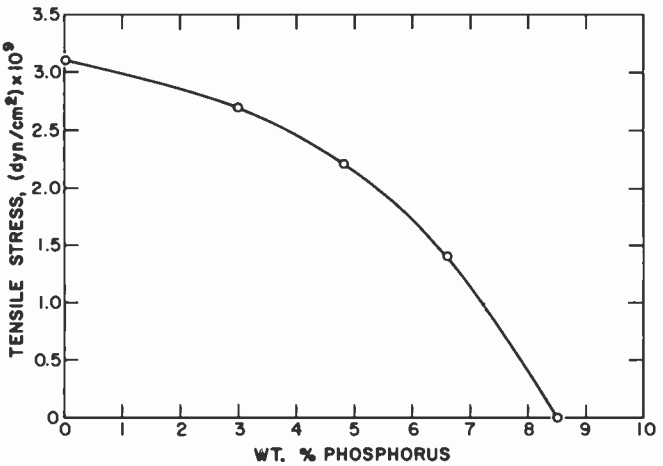


Fig. 11—Room temperature tensile stress versus wt % phosphorus for films deposited at 450°C at a rate of 1 μm/min. Deposition of these films was carried out in a continuous processing reactor (PWS-2000).

the aluminum.[1,52,53] The relationship of phosphorus content in 1-μm-thick PSG films deposited at 450°C and the room-temperature tensile stress is shown graphically in Fig. 11.

Layers of SiO_2 and of 2, 3, and 4 wt % phosphorus PSG were deposited on IC device wafers and examined for stress cracks. CVD processing was carried out in the rotary reactor under the usual conditions at 450°C, and the layer thicknesses ranged from 1.1 to 1.2 μm. Both linear bipolar IC's (CA3747) with large aluminum-metallized capacitor areas and CMOS IC's (CD4017A) were chosen for these

tests. The overcoat layers were delineated by photolithography and chemical etching to open the aluminum bond-pad areas and the grid lines. Microscopic examination showed that the highly stressed SiO_2 layer had cracked along the edges and in the interior of the large aluminum-metallized areas. Additional cracks formed along the entire edge of the circuit over the dense oxide. The glass layers containing 2, 3, or 4 wt % phosphorus exhibited no cracks, thus demonstrating that the incorporation of a relatively small amount of phosphorus in the glass can have a very large effect on preventing glass cracking.

5.7 Effect on Stress of Intentionally Introduced Water Vapor During CVD of SiO_2 and PSG Films

It has been demonstrated that substantial degrees of densification of CVD films can be achieved by prolonged heat treatments at 450°C in ambients containing water vapor.[2,4] To attempt to lower the tensile stress directly in the as-deposited layers, H_2O vapor was intentionally added into the CVD reaction chamber at a deposition temperature of 450°C.

Since H_2O is one of the reaction products when SiH_4 is oxidized, it was necessary to substantially increase the H_2O content to observe an effect. This was easily accomplished by passing the main N_2 carrier

Table 4—SiO_2 Films Deposited on Silicon in Dry and Wet Nitrogen

Substrate Deposition Temperature (°C)	Water Vapor Content (factor increase over that present from chemical reaction)	Deposition Rate (Å/min)	Stress (dynes/cm²)
350	0	1750	3.2×10^9
	4.2	1750	2.8×10^9
	0	500	2.5×10^9
	6.7	500	2.2×10^9
450	0	1000	2.8×10^9
	9.2	1000	2.4×10^9
	0	350	2.7×10^9
	14.5	350	1.7×10^9

gas through a fritted glass bubbler to saturate the N_2 with H_2O vapor at room temperature. Assuming a 50% oxidation of the SiH_4 in the reaction chamber, the H_2O vapor content was increased 9.2 times. O_2 could also be passed through a bubbler to further increase the H_2O vapor content.

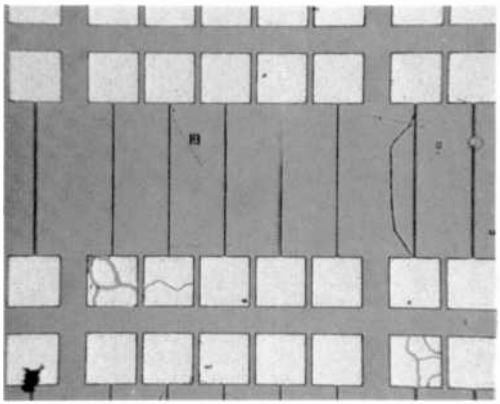
Tensile stress in the CVD SiO_2 films deposited on silicon wafers at 450°C by this technique was reduced from 3.4×10^9 dynes/cm^2 to values as low as 1.7×10^9 dynes/cm^2, as shown in Table 4. To further confirm that tensile stress was lowered by deposition in wet nitrogen, two CVD SiO_2 layers, one prepared with wet nitrogen, the other with dry nitrogen, were deposited. The substrates consisted of thermally oxidized silicon wafers with 1-μm-thick aluminum test patterns containing large metal areas, since CVD SiO_2 layers over aluminum are very susceptible to cracking. Subsequent to CVD deposition the samples were etched in hot (55°C) aluminum etch for 10 minutes to reveal cracks in the SiO_2 films (cracks or pinholes in the overlying glass will allow the etch to reach the metal, thus etching it away).[7] The samples having an oxide prepared with wet nitrogen had no cracks, while cracks were observed on the sample prepared with dry nitrogen. Both samples were then reheated at 450°C for 1.5 hours in nitrogen, cooled, and re-etched for an additional 10 minutes in the hot aluminum etch. Microscopic examination showed a few cracks on the sample prepared with wet nitrogen, while the sample prepared with dry nitrogen was severely cracked (Fig. 12). A summary of these tests is presented in Table 5. A scanning electron micrograph of the sample prepared with dry nitrogen, taken at ×2000 magnification at an incidence angle of 30°, is shown in Fig. 13. The aluminum film was etched away between 6 and 8 μm from the crack in the SiO_2 layer. Studies employing selective-etching techniques and SEM have shown that these stress-induced microcracks in SiO_2 layers deposited under "dry" CVD conditions over aluminum patterns do not extend beyond the aluminum area, but run across the aluminum patterns and along most of the SiO_2 layer top corner covering the edge of the aluminum pattern. The cracks are not nucleated by pinholes or other defects in the SiO_2 or aluminum films.

This same test was repeated using a 1-μm-thick PSG layer over 1-μm-thick aluminum patterns. Because PSG glass layers are under less tensile stress than SiO_2 layers as deposited, no cracks were observed on either the wet or dry nitrogen samples. However, by heating the samples to 525°C for 10 minutes and then giving the samples a hot aluminum etch, some cracks did appear in the PSG layer deposited with dry nitrogen, while none were observed on the sample prepared with wet nitrogen (Fig. 14). Composition analysis of the PSG films showed that the phosphorus content was not markedly affected by the use of wet N_2. The results thus indicate that under the same deposition conditions, CVD SiO_2 films or PSG films deposted with wet nitrogen carrier gas have lower intrinsic tensile stress than films deposited with dry nitrogen (Table 5).

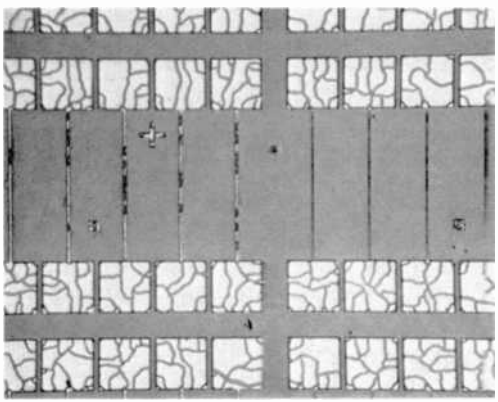
Table 5—SiO_2 and PSG Films Deposited on Aluminum Patterns In Dry and Wet Nitrogen

Sample	Water Vapor Content (Factor Increase Over That Present From Chemical Reaction)	Deposition Rate (A/min)	Visual Examination After CVD	Visual Examination After Post-Deposition Heat Treatment
SiO_2 Layer Deposited on 1μm-Thick Aluminum Pattern At 450°C	0	1000	Some Cracks	Severely Cracked
	9.2	1000	No Cracks	A Few Cracks
	14.5	350	No Cracks	No Cracks
PSG Layer Deposited on 1μm-Thick Aluminum Pattern at 450°C	0	1000	No Cracks	Some Cracks
	9.2	1000	No Cracks	No Cracks

The use of such films in the manufacture of semiconductor devices should result in higher yields and greater reliability, especially where the CVD oxide layers are used as an insulator or passivating glass, since glass cracking is a major cause of device failures and degradation.[1,9,52]



(a) Deposition of SiO_2 layer performed in wet N_2



(b) Deposition of SiO_2 layer performed in dry N_2

Fig. 12—Cracks revealed in a 1-μm-thick CVD SiO_2 layer deposited over an aluminum pattern, followed by a 450°C heat treatment and aluminum etching.

Infrared absorption spectroscopy of SiO_2 and PSG films deposited in the presence of water vapor have shown no larger quantities of included water in the film structure than is normally observed under dry conditions.

5.8 Effects of Deposition Rate on Stress for Films Deposited with Either Dry or Wet Carrier Gas

Room-temperature stress in 1-μm-thick CVD SiO_2 layers as a function of deposition rate was studied at deposition temperatures of 350° and 450°C for both dry and wet nitrogen carrier gas, with the following results.

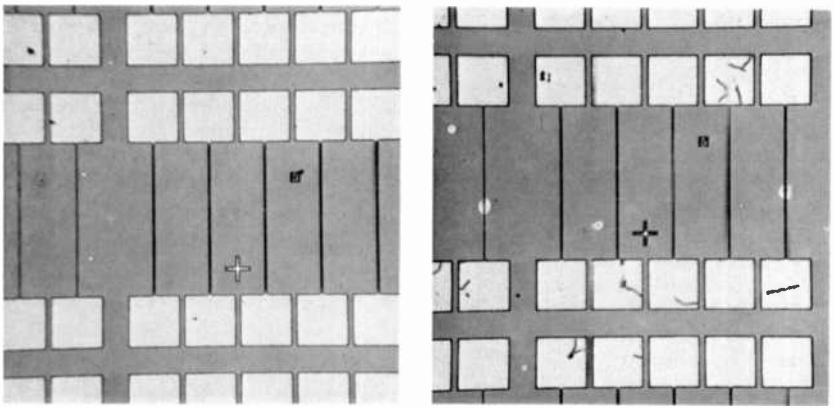
Fig. 13—Scanning electron micrograph of cracks in CVD SiO_2 over aluminum, ×2000, 30° incidence. Sample was etched in hot aluminum etch, resulting in removal of aluminum from the area adjacent to the cracks.

The stress in films deposited at 350°C with both dry and wet nitrogen carrier gas was found to be tensile and was essentially constant for deposition rates of 1000 to 2400 Å/min, while below 1000 Å/min the stress decreased as the deposition rate was decreased, as shown in Fig. 15 and outlined in Table 4.

The stress in films deposited at 450°C in both dry and wet nitrogen decreased as the rate was decreased from 5000 Å/min. For wet nitrogen carrier gas, the decrease in stress was larger than with dry carrier gas at deposition rates below 750 Å/min, as shown in Fig. 16. Again, all film stresses were tensile.

5.9 Stress Measurements of Films Deposited in Various CVD Reactors

A comparison of stress in CVD SiO_2 films deposited in four different



(a) Deposition of PSG layer performed in wet N_2

(b) Deposition of PSG layer performed in dry N_2

Fig. 14—Cracks revealed in a 1-μm-thick CVD PSG layer deposited over an aluminum pattern, followed by 525°C heat treatment and aluminum etching.

reactor systems, including several commercially available systems, was made. Deposition temperatures in the range of 400° to 450°C and deposition rates from 1000 to 10,000 Å/min were used; these were close to optimum operating conditions for each reactor system (in terms of deposition rate and thickness uniformity). The highest stress observed, 3.1×10^9 dynes/cm^2, was on samples prepared on the AMS-2000 model. The lowest stress observed, 2.7×10^9 dynes/cm^2,

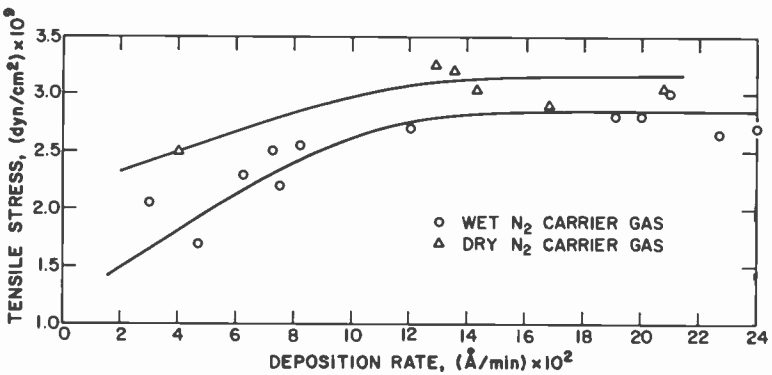


Fig. 15—Room-temperature tensile stress in SiO_2 films deposited at 350°C with either dry or wet nitrogen as a function of deposition rate. Additional details are presented in Table 4.

Table 6—Stress in CVD SiO_2 Films Deposited in Various Types of Reactors[2]

CVD Reactor System*	Deposition Temperature (°C)	O_2:SiH_4 Mole Ratio	Deposition Rate (Å/min)	Stress (dynes/cm²)
AMS-2000 Continuous Silox Reactor	410	15:1	1,060	3.1×10^9
PWS Model 2000 Vapor Deposition System (Standard nozzle used)	450	20:1	10,000	3.0×10^9
Rotox-60 Reactor	400	9:1	1,000	2.9×10^9
RCA Single-Rotation Reactor [3]	450	20:1	1,000	2.7×10^9

*For description of reactors and addresses of manufacturers, see Refs. [2] and [3].

was on samples prepared on the RCA designed rotary reactor. A description of the stress results and deposition conditions is given in Table 6.

The observed range of 2.7 to 3.1 × 10^9 dynes/cm² is actually a surprisingly small range for room-temperature stress of SiO_2 films on Si, considering differences in deposition conditions and equipment. On the other hand, since crack formation is a threshold type effect, with no cracks occurring until critical conditions are reached, small changes in intrinsic tensile stress can make large differences in the incidence of crack formation.

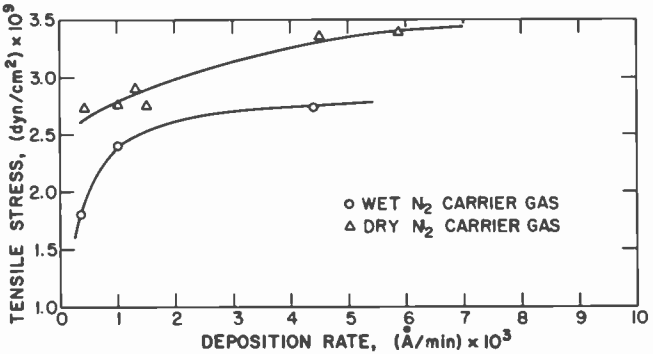


Fig. 16—Room-temperature tensile stress in SiO_2 films deposited at 450°C with either dry or wet nitrogen as a function of deposition rate. Most points shown are an average of several separate deposition experiments. Additional details are presented in Table 4.

5.10 Effects of Densification on Stress

Stress of a 2-μm-thick CVD SiO_2 film deposited on a silicon wafer was measured before and after thermal densification. Prior to densification the film was in tensile stress of 2.9×10^9 dynes/cm^2. After densification of the film at 1000°C in air for 30 minutes, the room-temperature stress became compressive with a value of 3.0×10^9 dynes/cm^2. Fig. 17 shows the profiles of the wafer before and after densification. The inverted profile indicates that the stress has changed from tension to compression.

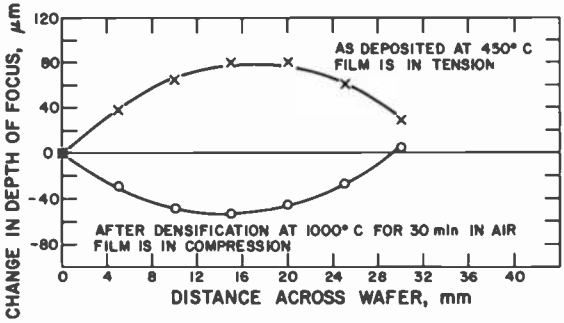


Fig. 17—Profiles before and after densification of a silicon wafer with a 2-μm-thick CVD SiO_2 layer.

PSG layers with very little stress at room temperature were deposited. The layers were 9400 Å thick and contained 8.5 wt % phosphorus. After deposition on both 190-μm and 63-μm-thick silicon substrates, no appreciable deformation of the substrate could be measured at room temperature, indicating absence of room-temperature stress. Upon densification of the glass layer at 1000°C for 15 minutes in oxygen, the layer was in compressive stress of 1.3×10^9 dynes/cm^2.

The lower value for room-temperature compressive stress in CVD PSG films after densification could be attributed to a lower coefficient of thermal expansion for PSG films than for SiO_2, to a lower annealing temperature for PSG films, or to a combination of these. While very little information is available on the linear coefficient of thermal expansion of PSG,[9,37,40] the SiO_2-P_2O_5 phase diagram[54,55] does contain a eutectic with a melting point below 1000°C, and phosphosilicates are known to have lower annealing temperatures. Thus the lower room-temperature compressive stress of the annealed PSG

films compared to SiO_2 films is attributed to the lower annealing temperatures of PSG films.

The effects of low-temperature (450°C) densification were examined for IC's with glass overcoatings and have been reported elsewhere.[1,2,4]

5.11 Stress and Cracking as a Function of Film Thickness

Stress as a function of film thickness was measured for CVD SiO_2 layers deposited at a constant rate at 450°C. A sequential deposition was carried out, and stress measured at intervals of 3200, 6400, 9600, 12,800, and 16,000 Å. A plot of stress versus film thickness is shown in Fig. 18. Stress remained relatively constant up to 16,000 Å. As the

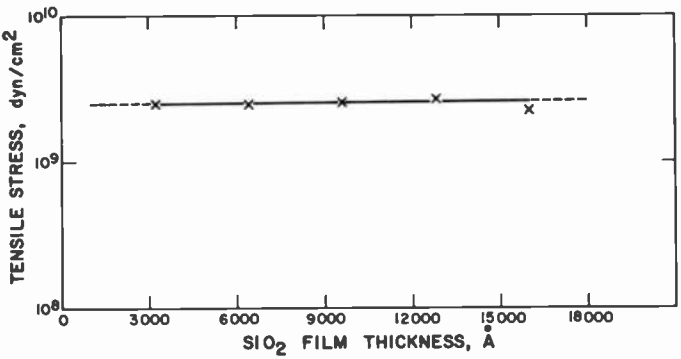


Fig. 18—Stress as a function of film thickness for CVD SiO_2. Deposition rate was held constant at 1300 Å/min.

thickness increases beyond 16,000 Å, cracks form and meaningful stress values cannot be obtained. The observed results imply that the stress is principally attributable to the SiO_2 film itself, rather than to a transitional layer at the deposited SiO_2–substrate interface or to the SiO_2–ambient interface.

Experiments were also conducted with SiO_2 films deposited with dry or wet nitrogen over aluminum-coated wafers to determine the onset of stress-induced microcrack formation as a function of SiO_2 film thickness. The aluminum was 5000 Å thick, and had been vacuum-evaporated on unheated silicon wafers that were previously thermally oxidized to a thickness of 5000 Å of SiO_2. The Al films were not patterned, so as to obtain an entirely planar test substrate. The SiO_2 films were deposited at a rate of 2000 Å/min in a rotary reactor

at 450°C with either dry or wet nitrogen to graded thicknesses ranging from 10,000 to 17,000 Å. The essential result of this experiment was the fact that onset of microcrack formation (along the sample edges) for the SiO_2 films deposited with dry nitrogen was at a thickness of 10,300 Å,whereas it was at 12,700 Å for the films deposited with wet nitrogen. This indicates that both film thickness and the presence or absence of excess water vapor during CVD are factors in stress-induced microcracks. The density of cracks increased with increasing SiO_2 film thickness, but remained less for the films deposited in wet nitrogen by a roughly constant thickness factor.

It should be pointed out that these critical SiO_2 crack induction thicknesses are relative and depend on the exact composition of the substrate material and its surface. For example, an alloyed aluminum film on silicon can be expected to give entirely different results than would an aluminum film of the same thickness deposited on oxidized silicon or on a bare silicon substrate wafer.

Tests with various types of integrated circuits showed that crack-free overcoating layers of PSG can be deposited in a rotary CVD reactor to thicknesses of at least 1.2 μm if the phosphorus content is 2 wt % and the film deposition rate does not exceed approximately 2000 Å/min. Thicker layers require higher phosphorus concentrations to avoid formation of defects due to stress. A layer of PSG containing 4 wt % phosphorus deposited in a rotary reactor at a temperature of 450°C over aluminum-metallized IC wafers to a thickness of 2.0 μm (plus a top layer of 0.1-μm SiO_2) still cracked, indicating that the layer thickness is excessive for this phosphorus concentration.

5.12 Stress Measurements at Elevated Temperature

The total stress measured at room temperature is a combination of the intrinsic stress in the film as deposited and the stress arising as a result of mismatches in the thermal coefficients of expansion of the CVD film and the silicon substrate. Typically, CVD SiO_2 or PSG films are in tension as deposited, for example, at 450°C. As the sample is cooled to 25°C, the coefficient of expansion of SiO_2, being lower than that of silicon, results in some reduction in the net tension in the CVD film.

An experiment was conducted whereby stress at the deposition temperature of 450°C for a 1-μm-thick layer SiO_2 film on silicon substrate was measured. The focal-point method[38] was used for this experiment, with the focal point measured at both 450°C and at room temperature. A room-temperature determination of stress was also made by the profiling method, as a comparison. Stress at 450°C was

found to be 4.7×10^9 dynes/cm^2, while at room temperature the stress was 2.9×10^9 dynes/cm^2. Room-temperature stress measured by the profiling method was 2.7×10^9 dynes/cm^2. Thus, stress in this particular CVD SiO_2 film was approximately 60% greater at the deposition temperature of 450°C than at room temperature.

A similar experiment was conducted on a 1-μm-thick PSG layer containing 8.5 wt % P. Stress at the 450°C deposition temperature was measured to be 2.4×10^9 dynes/cm^2, while room-temperature stress was zero.

5.13 Comments on Stress and Its Measurement

When CVD systems are producing deposited SiO_2 or PSG films that are near the threshold for crack formation, relatively small changes in the operating conditions can, by producing small changes in intrinsic stress in deposited films, result in large differences in the incidence of crack formation. The data on dry versus wet oxides provide several illustrations of the potential effects of small changes in stress in deposited films.

It should be pointed out that the precision of many stress measurement methods is substantially better than their absolute accuracy. We believe the profile focus method and the two crack formation methods provide the capability of detecting relatively small differences in room-temperature stress in deposited CVD films due to variations in deposition conditions. They thus provide techniques that can permit improvements in vapor-deposition conditions and equipment, and can provide semiquantitative information on the effect of the more significant vapor-deposition conditions on intrinsic tensile stress of CVD films.

The differences in stress values calculated by the focal-point method at 450°C versus room temperature can be used to provide an indication of the linear coefficient of thermal expansion of the deposited PSG film relative to SiO_2. The stress difference for SiO_2 was 1.8×10^9 dynes/cm^2, whereas the stress difference for the PSG containing 8.5% P was 2.4×10^9 dynes/cm^2. Since the calculation for the measurements performed at 450°C were made using the room-temperature values for (111) silicon (Glang's values), it is recognized that changes in Young's modulus or in Poisson's ratio of Si with temperature could change the focal point. On the other hand, amorphous SiO_2 has a much lower coefficient of expansion than Si, and thus cooling of wafers with deposited SiO_2 films on Si would reduce the tensile stress, as was observed. (The data of Jacodine and Schlegel[51] would lead to a predicted change in stress for SiO_2, from 450°C to room temperature,

of about 1.1×10^9 dynes/cm^2.) Thus the linear coefficient of thermal expansion of PSG films containing 8.5 wt % phosphorus can be considered to be approximately equal to that of amorphous SiO_2. The linear coefficient of thermal expansion of PSG compositions of the type used for passivation of silicon devices, such as PSG containing 3 wt % P, would thus be approximately equal to that of CVD SiO_2 containing no phosphorus.

6. Studies of Defects in Glass Films

Defects of various types in glass passivation overcoats are frequently introduced during CVD of the films, or during processing steps associated with glassing, such as surface preparation and photolithography. These film defects can be categorized into two main groups: (1) localized structural and compositional defects, and (2) nonlocalized chemical and physical defects. Several causes of defect generation have already been mentioned in preceding sections and are summarized below, together with additional information and some experimental data.

6.1 Localized Structural and Compositional Defects

Particulate contaminants (dust or reaction products) in the gas or vapor streams or on the substrate surface during chemical vapor deposition interfere with film nucleation and proper growth, resulting in voids, thin spots, partial or complete pinholes, or hillocks. Particulate impurities that become embedded in the film constitute a potential device failure due to local weakening of the dielectric strength.

Pinholes in the films can also be caused by problems in photolithographic processing if the photoresist protects the film incompletely, or if the etchants used in the chemical patterning process penetrate through pinholes or thin spots in the resist coating itself.

Gas bubbles that weaken the dielectric strength of an insulator may form during chemical vapor deposition in the presence of nucleating particulate contaminants. Unacceptable topographical defects, such as excessive surface roughness, may also arise during film deposition under incorrect process conditions.

Microfractures are a very common and important mode of a localized defect caused by excessive stress (see Section 5). Other localized defects include embedded foreign particles, microcrystallites, or precipitates caused by reactions in the solid state. Oxides and glasses may devitrify in local regions under certain conditions, and may deleteriously affect film integrity and dielectric strength.

The topography of the substrate being coated with a dielectric film may cause defects in the film deposit, such as thin spots over sharp edges or film discontinuities in corners at the base of steep steps that may lead to electrical short-circuits. A review has been presented elsewhere of IC failure mechanisms[50] as has a discussion of methods specifically designed to improve the reliability of electron devices by optimized coverage of surface topography.[49]

Surveys of analytical methods for detecting and characterizing localized defects in dielectrics[45] and of failure analysis of oxide defects on IC's[56] have been published recently, as well as studies of the effects of induced localized passivation layer defects[57] and of localized defects in deposited glass layers.[43]

6.2 Nonlocalized Chemical and Physical Defects

Chemical imperfections include deviations in film composition, which may be nonstoichiometry in the case of single-component dielectric films, or incorrect percentages of one or several components in a binary or multiple component material. Chemical impurities in the bulk or on the surface of a film are another common chemical imperfection that may deleteriously affect device performance due, for example, to current conduction across the contaminated film surface. Incorrect layer composite structures, caused by inappropriate sequence, thickness, or composition of various dielectric layers, may give rise to excessive stresses and/or a variety of other problems, such as poor adherence, instability in composition, or intolerable degrees of hygroscopicity (in the case of excess B_2O_3 or P_2O_5 in a glass).[52,58,59] These basic causes may deleteriously affect important mechanical and electrical film properties, such as thermal expansion and stress, bulk and surface resistivity, dielectric strength and dissipation, charge density, and polarizability.

Of particular concern in IC glassing is the presence of residual stress in the films, which may lead to cracks in the glass. Thermal expansion is one major factor determining the magnitude and the sign of the residual stresses at interfaces between dielectric layers or at the interface between a dielectric and the metallization, and, of course, between the thermal SiO_2 primary passivating layer and the thick silicon substrate crystal. A summary of stress data for various dielectric films of interest here has been presented elsewhere.[60]

The stress inversion data for CVD SiO_2 reported illustrate the complexity of the mechanical stresses inherent in device wafers. However, variations in CVD processing parameters and subsequent heat treatment of the amorphous dielectric films can significantly re-

duce these stresses. For example, for a given growth rate and thickness, the tensile stress is greatest for pure SiO_2 films and decreases with increasing P_2O_5 concentration in the glass. Similar results are observed with borosilicates and other CVD glass films. Temperature and film deposition rate are also factors that affect the stress level in a complicated manner.

Microfractures can be caused by stresses between the dielectric film and the substrate or between different types of films. Stress in films may develop during deposition processing, pattern etching, or heat treatments, especially if the linear thermal expansions of the components are mismatched. Cracks may form, particularly during thermal shocking preceding or following high-temperature processing, excessive thermal contraction on cooling, or temperature stress cycling and life testing of devices.

6.3 Photolithographically Caused Glass Damage

Some pinholes and cracks can be generated by the contact printing operation[1,9] or by impact during chip handling.[43,45,61] When the photomask comes in contact with the glass-passivated aluminum pattern, large pressures occur at points of contact. The result is that the aluminum flows slightly and the glass may crack. Hillocks present in the aluminum also flatten and cause glass damage.

To investigate this mechanism, a silicon wafer with a glassed aluminum pattern was sequentially etched in hot aluminum etch to reveal cracks and pinholes following contact printing steps. The etching studies showed that more cracks and pinholes developed each time the glassed pattern was brought into contact with the photomask. The experiment was carried out by starting with an oxidized silicon wafer with an aluminum test pattern overcoated with a CVD PSG layer (5000 Å 2.5 wt % P PSG plus 2200 Å SiO_2 cap) and etched in aluminum etch (6 min, 55°C); microscopic examination showed that no structural defects were present in the glass. The wafer was photoresisted and brought into contact with a photomask by automatic exposure in the vacuum contact printing mode of a typical commercial wafer aligning instrument. The photoresist was then removed by careful solvent stripping, and the previously run aluminum etch test repeated. Microscopic examination revealed the presence of several defect sites that had been caused clearly by the automatic contacting during the photolithographic printing operation. The appearance of typical glass defects from this experiment is shown in the photomicrographs in Fig. 19.

It should be pointed out in this connection that our evaluation of passivation overcoats on commercial IC's[7] has shown that in a substantial portion of the integrated circuits manufactured in the last several years, the passivation layer contains pinholes, cracks, or a combination of these; a number of publications also confirm this finding.[43,45,50,62-64] The more common class was pinholes in the central regions of aluminum lines. Another type observed was pinholes along the edge of the delineated metal lines.[45] The edge pinholes are attributed to inadequate coverage of metal edges by the photoresist, and can generally be avoided by the use of thicker photoresist layers or improved photoresist application techniques. Those pinholes that occurred in the central areas of delineated lines are, to a large extent, believed to be attributable to the presence of hillocks in the alumi-

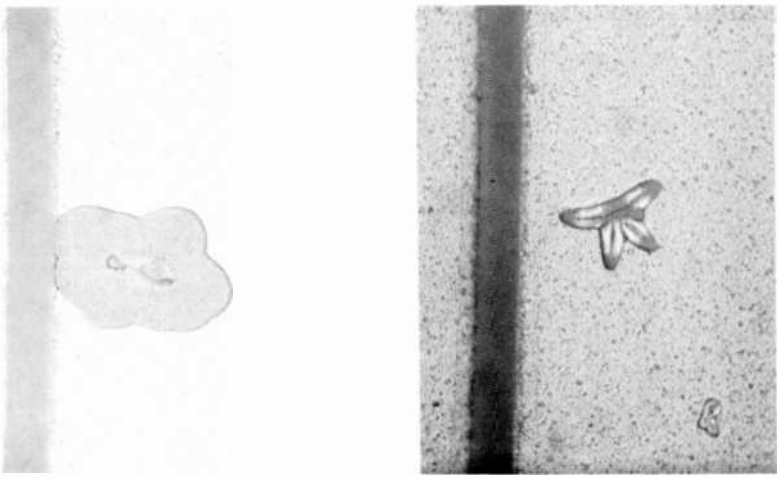


Fig. 19—Typical glass damage over aluminum caused by photomask automated vacuum contact, as explained in text. Defects were made visible by aluminum demarcation etching (275× magnification).

num[9,43] which occur because of recrystallization of the aluminum during the contact alloying step. It should be noted that even if a hillock is completely covered with dielectric during the subsequent step of deposition of the passivation layer, the hillock may not be adequately covered by photoresist, the photoresist may be pushed away from the peak of the hillock during contact printing, or the contact printing step may fracture the dielectric over the hillock. Any of these three conditions, or a combination, will result in a pinhole through the passivation layer, exposing a region of aluminum and

leading to potential reliability problems[9] and impairment of product yield.[65]

6.4 Analytical Control Methods

Practical methods and measurement techniques suitable for setup and in-process control of production-type CVD passivation work, as well as for detection of structural layer defects, are outlined in Table 7. All of these chemical, optical, electrical, and mechanical test methods have been discussed and literature sources have been referenced in a recent survey paper.[9] Recent improvements we have made in methods for PSG analysis, especially x-ray fluorescence,[1] and chemical-etch-rate measurement techniques[7,8] have been discussed elsewhere.

7. Conclusions

The effects of various deposition conditions on the properties of CVD PSG films have been studied in detail, and the relative importance of 12 critical conditions has been established. It has been concluded that the most important conditions to control, in declining order of importance, are: substrate temperature of deposition, oxygen-to-hydride ratio, hydride flow rate, silane-to-phosphine ratio, and nitrogen flowrate. Other important factors examined include reactor geometry, wall temperature of the reactor, gas additives, system cleanliness and gas purity, substrate surface characteristics, and substrate geometry and topography.

The essential effects of CVD key parameters on PSG film deposition rate, phosphorus content, and intrinsic film stress are shown in Table 8. This table allows one to predict, at a glance, what results can be expected on combining the various parameters, or how to compensate for an effect by increasing or decreasing the relative magnitude of some of the other factors. Most of the observed effects have been explained and compared with data published in the literature.

Most of the CVD studies reported were carried out by batch processing using a pilot production-type vertical rotary deposition system. Comparative experiments with SiO_2 and PSG films were conducted using representative commercial production-type continuous processing systems of the more important types. Even though the principle of operation may differ greatly for various types of systems, the basic CVD parameters underlying oxide and glass film formation by gas phase oxidation of the hydrides at temperatures below 500°C

Table 7—Measurement Techniques for Setup and In-Process Control of Production-Type CVD Passivation-Glass Deposition

Characteristic	Substrate to be Used	Measurement Technique	Deposition Condition to be Adjusted as Required
Thickness	Si wafer	Interferometric technique; stylus-type instrument	Time of deposition
Density	Si wafer	Etch rate (as deposited)	Deposition rate, deposition temperature
Phosphorus content	p-type Si wafer	Sheet resistivity after high temperature bake; etch rate after densification; x-ray fluorescence analysis	PH_3/SiH_3 ratio
Total stress	0.14-mm-thick Si wafer	Wafer warpage by optical microscopy	Deposition rate, deposition temperature, SiH_4/O_2 ratio
Interfacial stress	0.6- to 1-mm-thick Si wafer	Surface temperature measurements; pyrometry	Deposition temperature
Surface topography	Si wafer	Nomarski interference contrast microscopy; stylus-type instrument	Substrate cleanliness, system maintenance, cooling of system parts above the substrate
Pinholes	Patterned Al on oxidized Si wafer	Preferential Al etch, inspect	Substrate conditions, system maintenance
Cracks	Patterned Al on oxidized Si wafer	Inspect, Al etch, inspect, heat treat, Al etch, inspect	Deposition rate, deposition temperature, SiH_4/O_2 ratio
Edge coverage	Patterned Al on oxidized Si wafer	SiO_2 etch, Al etch, inspect	Reactant flow rate, edge topography of substrate

Table 8—Effects of CVD Key Parameters for Preparing PSG Films

DIRECTION OF ARROWS INDICATES RELATIVE INCREASE OR DECREASE

↗↘ STRONG; ≺ SLIGHT; → NONE

CVD PARAMETERS	EFFECTS ON FILM		
	DEPOSITION RATE	PHOSPHORUS CONTENT	INTRINSIC STRESS
HYDRIDE FLOW RATE $\frac{SiH_4 + PH_3}{Time}$ ↑	↗	→	↗
HYDRIDE RATIO $\frac{PH_3}{SiH_4}$ ↑	↗	↗	↘
OXYGEN RATIO $\frac{O_2}{SiH_4 + PH_3}$ ↑	∩	∧	↗
DEPOSITION TEMPERATURE T ↑	H / → / L	↘	↘
DILUENT GAS FLOW RATE $\frac{N_2}{Time}$ ↑	∩	→	→

H = HIGH, L = LOW OXYGEN RATIO

are, in principle and often semiquantitatively, applicable to all systems.

The critical factors determining PSG composition and film quality must be controlled and optimized for a given CVD system by analysis of the film product obtained.

The CVD process should be directed in a fashion conducive to heterogeneous gas-phase nucleation to produce clear, glassy films free of defects. Homogeneous gas-phase reactions produce particulate contaminants and must be suppressed by application of the techniques discussed.

Even though the exact reaction mechanism of film formation is quite complex and is influenced by many variables, the optimized CVD of high-quality SiO_2 and PSG films for IC overcoat passivation is a process well suited for large-scale production.

In addition, a practical method has been developed for measuring stress in CVD films deposited on silicon wafers; the method is based on measuring the profile bow of a coated substrate wafer. It requires no special fixtures for the wafer during deposition and is thus applicable to any type of deposition system. A second method is valuable for comparison of relative stress in CVD passivation films on various substrates including aluminum-metallized IC wafers. In this method, microcracks per unit area are counted after CVD and after thermal stress induction at increasing temperature levels from 450° to 550°C. Both methods provide the capability of detecting relatively small differences in room-temperatures stress in deposited CVD films due to variations in deposition conditions, and can provide semiquantitative information on the effect of the more significant vapor deposition conditions on intrinsic tensile stress of CVD films.

A correlation has been demonstrated between intrinsic stress in deposited films and susceptibility to cracking during deposition or during subsequent exposure to thermal stress conditions, particularly at processing temperatures higher than the deposition temperature. Excessively low phosphorus content in CVD films was correlated with excessive intrinsic tensile stress leading to crack formation. This is the main reason, next to the alkali gettering effectiveness, for our conclusion that CVD phosphosilicate glass, deposited under controlled conditions, offers significant advantages over SiO_2 for passivation of integrated circuits.

A new technique for lowering stress in CVD SiO_2 and PSG films has been developed. By depositing films using moisture-containing nitrogen carrier, we have obtained films with lower stress.

A number of generalizations can be made concerning the effect of deposition conditions on stress in CVD films. In particular, lower

stress is attained with lower deposition rates, with higher deposition temperatures, and with higher phosphorus content. In some cases, lower oxygen/silane ratios result in lower stress levels. Relatively small changes in the magnitude of the residual stress at room temperature can correspond to relatively large differences in the incidence of cracks over large metal areas or along the edges of delineated metal films.

Since cracking at the edge of metal films depends on many factors, including the angle of the edge of the delineated metal areas, the size of the metal area, the thickness of the metal film, and the nature of heat treatments after metallization, an appropriate technique for production control purposes is to perform selective aluminum etch tests after appropriate heat treatments of the wafer. If essentially no additional microcracks form as a result of a heat treatment step (50°C or more above the maximum processing temperature of the particular device type under study), it can be concluded that intrinsic stresses during CVD were not excessively high.

The differences in stress values calculated by the focal point method at 450°C versus room temperature was used to estimate the linear coefficient of thermal expansion of CVD PSG films relative to SiO_2. The linear coefficient of thermal expansion of PSG compositions of the type used for passivation of silicon devices was concluded to be approximately equal to that of CVD SiO_2 containing no phosphorus.

Types and causes of structural and compositional defects in glass passivation layers were briefly examined with respect to CVD glassing and associated processing steps. Experimental results have been presented that demonstrate the cause of damage in glass layers over aluminum metallization during the photolithographic contact printing operation. The types of defects most commonly encountered in passivation overcoats on commercial IC's have been noted, and their relationship to device reliability pointed out.

Finally, practical analytical methods and measurement techniques suitable for setup and in-process control of CVD passivation layers, as well as for detection of structural layer defects, have been outlined as a reference.

Acknowledgments

The authors wish to thank R. D. Vibronek for capable technical assistance in the CVD work and etch rate measurements, B. L. Goydish, J. Sabo, and L. R. Schneid for wet chemical analysis, A. Decker for gas mass spectrometry, H. H. Whitaker for atomic absorption analysis, and R. Paff for x-ray fluorescence analysis. We also are indebted to

W. Bösenberg for making CVD production equipment available to us for testing, and to W. E. Ham and J. L. Vossen for critically reviewing parts of the manuscript.

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Densification of Vapor-Deposited Phosphosilicate Glass Films*

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Abstract—The kinetics of densification of chemically vapor-deposited (CVD) phosphosilicate glass films of various compositions has been studied for a variety of treatment conditions, with emphasis on temperatures of 450°C and below. It is shown by quantitative etch-rate measurements that significant degrees of film densification can be readily achieved at 450°C in relatively short times (5–10 hours) by using water vapor as a catalyst. The process is compatible with silicon integrated circuits metallized with aluminum. The rate of densification at room temperature has been established for dry and for humid ambients over periods of several thousand hours.

Densification at high temperature (800°C) diminishes in relative effectiveness as the phosphorus concentration in the film increases and decreases the etch rate drastically within minutes; beyond 10 minutes, it decreases logarithmically with time at a very low rate. Application of high-temperature densification is of practical importance for determining film composition by etch-rate measurements, and for enhancing the sensitivity of infrared absorption spectroscopic analysis by improving the spectral resolution of the characteristic P = O absorption band.

1. Introduction

The physical properties of oxide and silicate glass layers deposited at low temperature can generally be improved by a densification treat-

* This work was in part supported by the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-74-C-5146.

ment. In the absence of aluminum metallization, this process can be readily carried out by exposing the coated wafers to a temperature of 800°C for a few minutes.[1–4] However, for devices where such layers are deposited as an overcoat over aluminum metallization (as in the typical and important cases of most IC's and multilayer interconnect devices), it is impossible to heat the devices above the Al-Si eutectic temperature of 577°C without causing excessive and damaging alloying of the aluminum. A practical densification temperature of 450°C has been found safe, but requires thousands of hours to attain a satisfactory degree of densification, unless the process is catalytically accelerated. In this paper we report experimental results of studies directed toward the development of a practical process to achieve this. Chemical-etch-rate measurement was the primary technique used to monitor the rate of film densification because of its sensitivity and convenience.

Films of CVD SiO_2 are known to be densifiable at low temperatures.[4–7,12] As far as silicate glasses are concerned, we previously reported that for vapor-deposited borosilicate glass films, low-temperature catalytic densification involving use of water vapor in the furnace ambient makes it possible to improve the film properties to the point where they approach those of the bulk glasses,[6] but no data were available for PSG films. We have now found that, under similar conditions, a substantial degree of densification can be attained with CVD films of PSG in a reasonable period of time (on the order of several hours) at temperatures as low as 450°C without damage to the aluminum metallization, the devices, or the structural or chemical properties of the glass itself.

The results of exploratory studies using atomic hydrogen or ultraviolet radiation are briefly presented, although these agents have proven less effective than thermal treatments in the presence of water vapor. Atomic hydrogen is known from solid-state studies[8] to be a highly reactive species that could well be capable of inducing beneficial changes in the glass. Structural changes and volume compaction have been shown to occur on SiO_2 layers bombarded with ions and electrons.[9] Furthermore, it has been recently reported that substantial degrees of stress relief in silicon oxide (SiO) films deposited by reactive sputtering can be attained by ultraviolet irradiation.[10]

Measurements in the present work were confined to isothermal etch-rate determination to detect changes in film density. Infrared absorption spectra were taken in several instances to monitor structural changes. Some degree of stress release and densification occurs under storage at room temperature, as is shown. High-temperature

(800°C) densification is important for analytical consideration and will be noted briefly in this context.

2. Experimental Techniques

2.1 Film Deposition

Uniform PSG films of several compositions were deposited in the single-rotation reactor and by the CVD techniques described elsewhere.[11–14] Polished and chemically cleaned wafers of single-crystal silicon were used as substrates. For infrared absorption measurements, float-zone-refined, oxygen-free high-resistivity (100 ohm-cm) silicon slices of 0.65-mm thickness were used; these wafers were polished on both sides and had an infrared transmission in the 670 to 4000 cm^{-1} wavenumber range of 60%. Aluminum-metallized device wafers with linear bipolar IC's (CA3747) and CMOS IC's (CD4017A) were included in the deposition runs. Each run consisted of an assortment of, typically, seven wafers of 5 cm diameter to produce a sufficient number of samples of identical films for different tests.

Films for thermal densification studies were deposited at a deposition temperature of 450°C. The rate of film deposition was 2000 Å/min, and the oxygen-to-hydride ratio was kept constant at 20:1. Film thicknesses of 1.0 to 1.2 μm were deposited. Films of SiO_2 used for comparison tests were deposited under the same conditions. Films for the UV irradiation and atomic hydrogen experiments consisted, in addition to those above, of thinner layers (2000 to 3000 Å) deposited at 350°C to increase the sensitivity of the tests.

2.2 Thermal Densification Treatments

All low-temperature thermal densification experiments were carried out at 450° ± 3°C in resistance-heated quartz tube furnaces with quartz substrate holders. The dimensions of the quartz tubes were 5.1 cm I.D. × 100 cm length, with constricted end caps to prevent backflow of air. The ambient gas flow and water vapor conditions used are listed in Table 1. The moist gases were prepared by passing the carrier gas through a fritted-glass-filter gas wash bottle maintained at 25° to 26°C. Steam was generated in an all-quartz boiling flask with ground connector joints and was introduced undiluted into the furnace tube.

In the first series of tests, 3.8 wt % phosphorus PSG films were heated in moist forming gas (10 vol % H_2 + 90 vol % N_2) and in steam for periods ranging from 90 seconds to 100 hours.

In the second series of tests, films of SiO_2, 2.1 wt % phosphorus PSG, and 3.0 wt % phosphorus PSG were heated in all four ambients listed in Table 1 for periods of 0.1 to 10 hours.

High-temperature densification treatments were carried out in a furnace as described above, using dry nitrogen as the ambient.

Table 1—Ambient Conditions During Thermal Densification at 450°C

Nominal Ambient	Carrier Gas Purity (%)	Gas Flow Rate (cm^3/min)	Water* Evaporation Rate (cm^3 liquid/min)
Dry N_2†	99.9995	650	0
Moist N_2	99.9995	650	0.002‡
Moist (10% H_2-90% N_2)	>99.996	700	<0.002‡
Steam*	—	0	5.8

*Water used was deionized and distilled.
†High-purity grade; water content 1 ppm.
‡Water source at 25 to 26°C.

2.3 Densification Treatments under UV Irradiation and in Atomic Hydrogen

The radiation source used consisted of a mercury arc lamp operated at 1750 W and was positioned in front of a concave reflecting mirror. The emitted radiation was in the wavelength range of 180 to 1400 mμ, and was collimated by two pairs of plano-convex quartz lenses. One half of each coated wafer was shielded from UV with a half-wafer of silicon placed on top of it. Irradiation was conducted for 65 hours at 47°C in room air and also at 450°C in air for 20 hours.

Densification treatments in atomic hydrogen were carried out with partly shielded film samples identical to those described in the UV tests. They were exposed to atomic hydrogen plasma generated by an rf glow discharge in 30 vol % H_2 plus 70 vol % Ar at a pressure of 100 mm at a substrate temperature of 300°C. RF potentials of 350 V for a period of 3.25 hours and also of 150 V for 6.5 hours were used.

Details of these experiments are described elsewhere.[12]

2.4 Changes in Film Properties during Room-Temperature Storage

All PSG films were stored in desiccators over a drying agent (activated silica gel or Drierite*) at room temperature. Films of SiO_2 were

* W. A. Hammond Drierite Co., Xenia, Ohio.

stored under the same dry conditions, and also in room air of high relative humidity. Film analyses were carried out at intervals, typically, from 15 minutes after completion of film deposition to several thousand hours of storage.

3. Film Analysis

The composition of the PSG films was determined by etch-rate analytical techniques[11,12,15] using the calibration curves presented in Fig. 1. The relative degree or rate of densification effectiveness was deter-

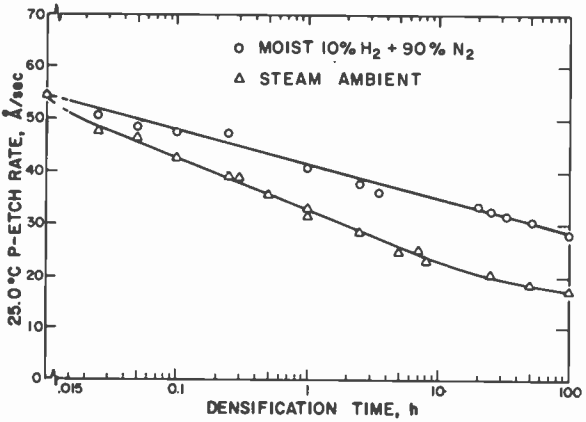


Fig. 1—Etch rate of a 3.8 wt. % phosphorus PSG film versus densification time and ambient at 450°C.

mined by chemical-etch-rate measurements initially and after various periods of treatment. The changes in the isothermal etch rate of CVD oxide or glass film of constant composition are a very sensitive measure of the relative changes of film properties reflected in the relative film density. The etch rate decreases as the density increases. Analysis was carried out by partly masking each heat-treated sample with wax, followed by measurement of the etch-time end point[16] in P-etch [2 vol HNO_3 (70%) + 3 vol HF (49%) + 60 vol H_2O][17] at 25.0° ± 0.2°C. The wax was then stripped and the film thickness measured by interferometric techniques using the film wedge formed along the masked area. Selected samples were checked by ellipsometric measurements and by profilometric techniques using a Talysurf.* The

* Taylor-Hobson, Ltd., England.

etch rate was calculated in Å/sec and plotted versus the densification time to obtain the rate of change.

Primary calibration of phosphorus concentration in PSG for all our analytical work was based on wet-chemical colorimetric analysis utilizing ammonium molybdate reagent. For this purpose the films were first dissolved in HF solution followed by elimination of all dissolved silicon to prevent its interference in the molybdate reaction. Two or three colorimetric tests were made per sample to obtain an average value.

Infrared absorption spectra were obtained with a double-beam spectrophotometer using the uncoated half of the identically heat-treated silicon wafer in the reference beam to compensate for lattice absorption of the silicon. Evaluation of IR frequency shifts and absorbance ratios of representative absorption bands was carried out by techniques reported previously.[3,4,6,18]

Electrical measurements of the IC samples were done by conventional techniques.[12]

4. Experimental Results and Discussion

4.1 Thermal Densification at 450°C

The etch-rate results for the first series of densifications in moist forming gas and steam for heat treatment periods of 90 seconds to 100 hours are presented graphically in Fig. 1. The resulting semilog plots demonstrate that densification of PSG films in steam for 1 hour decreases the etch rate to 0.58 R_o, where R_o is the initial etch rate, and to 0.38 R_o in 25 hours. The etch rate decreases uniformly with the logarithm of time up to about 10 hours, and then decreases more slowly. In wet forming gas, the corresponding values to which the etch rate decreased are 0.75 R_o and 0.60 R_o, respectively. For comparison, high-temperature densification at 800°C (15 min, N_2) decreases the etch rate to about 0.31 R_o (longer heat periods at 800°C have no significant additional effect).

Infrared absorption spectra of samples from the same series, taken after 11 time intervals over a heating period of 100 hours, showed only small changes from that of the initial film. Changes in both frequency and net absorbance were measured at the positions of maximum absorption of hydrogen-bonded SiOH groups at about 375 cm^{-1}, physically adsorbed H_2O in the range of 3400 to 3300 cm^{-1}, P = O at 1335 to 1330 cm^{-1}, Si–O at 1080 to 1060 cm^{-1} and its secondary at 830 to 800 cm^{-1}. The important results are the demonstration that (1) neither moist H_2-N_2 nor steam at 450°C introduce additional

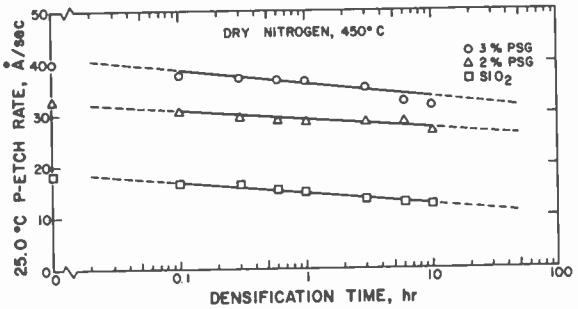
water into the films (in fact, some drying appears to occur); (2) the absorbance intensity of the P = O band remains constant, indicating that no loss occurs during heating; and (3) the spectral resolution of the P = O band is markedly improved after 5 hours at 450°C, similar to the effects observed after high-temperature (800°C) densification discussed in Section 4.4. Frequency shifts of absorption maxima were too small (within the error of analysis) to resolve quantitatively; however, the most pronounced changes appear to have occurred in the first 3 minutes of humid heat treatment at 450°C. The frequency of the secondary Si–O band shifted from an initial wave number of 830 cm^{-1} to 810 cm^{-1} for moist forming gas, and to 805 cm^{-1} for steam, and then remained essentially constant to 100 hours.

The samples densified for 100 hours were perfectly resistant to both water adsorption and phosphorus leaching; no changes were observed in the IR spectrum after 60 minutes boiling in deionized and distilled water.

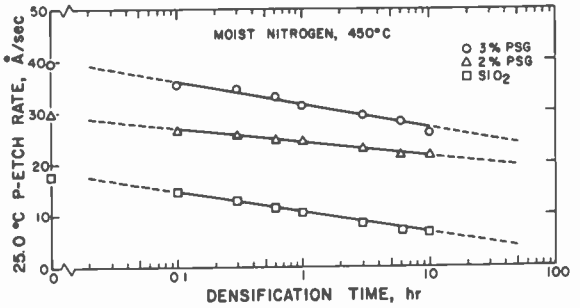
Separate samples of uniform, 1.0 μm-thick films on polished silicon substrates were prepared for measuring changes in the refractive index and the film thickness as a function of heat treatment. Ellipsometric measurements of the refractive index were taken at a wavelength of 5461 Å, and at an angle of radiation incidence of 70°. The films were assumed to be nonabsorbing and the optical constants of the silicon were taken to be 4.05 for the real part of the refractive index and 0.28 for the imaginary part. These measurements showed that a PSG film of 5.1 wt % P as-deposited at 450°C had a refractive index of 1.445. Heat treatment in steam at 450° for 10 hours increased this value to 1.454, indicating an increase in film density. Exposure of the film to 800°C in nitrogen for 15 minutes increased the refractive index further to 1.465. Films of CVD SiO_2 prepared under similar conditions had an initial refractive index of 1.436; 10 hours heating in steam increased this value to 1.459, and 15 minutes heating at 800°C in nitrogen led to 1.464.

Absolute thickness measurements of these PSG and SiO_2 samples by stylus techniques showed a decrease of 7.2% in the film thickness after the 450°C-steam heating for 10 hours. The 15 minutes heating at 800°C decreased the film thickness by 9.9% from the as-deposited value. This relatively small additional decrease of 2.7% in film thickness over that resulting after the 10-hour steam treatment at 450°C demonstrates the substantial degree of densification achieved by the low-temperature treatment. For comparison, the CVD SiO_2 films heated at 450°C for 10 hours in steam decreased in film thickness by 7.9%; this slightly greater degree of densification would be expected for films with lower phosphorus content.

The second series of thermal densification experiments was carried



(a)



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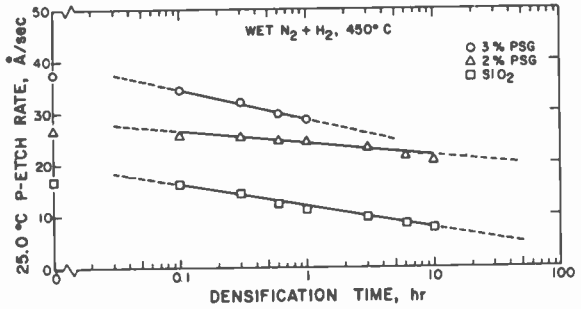
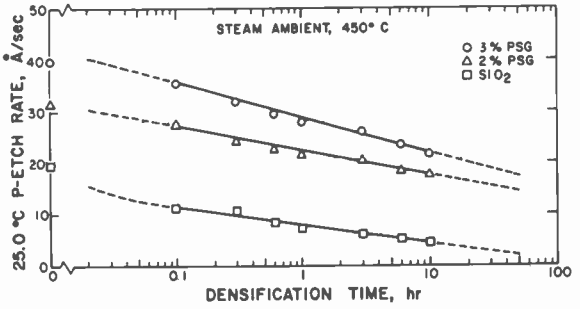


(c)



(d)

Fig. 2—Etch rate of SiO_2 and PSG films versus densification time at 450°C in (a) dry nitrogen, (b) wet nitrogen, (c) moist forming gas, and (d) steam ambient.

out under all four conditions listed in Table 1 using films of SiO_2, 2.1 wt % phosphorus PSG, and 3.0 wt % phosphorus PSG. All three types of films were heat-treated simultaneously for direct comparison. Etch-rate measurements were done after treatment periods of 0.1 to 10 hours, periods of time that are of practical interest in device processing. The results obtained are presented in Fig. 2a–d. The initial etch rate (time zero) is the etch rate just before the start of each densification experiment; it varies slightly for each type of treatment because the samples had to be stored for various lengths of time until use. The etch rate of all samples decreases linearly with the logarithm of heating time for all four ambient conditions. The rate of decrease depends on both the ambient conditions and film type. Moist nitrogen and moist forming gas effect a considerably greater rate of decrease than does dry nitrogen. Steam ambient, in turn, effects a still greater rate of decrease than the moist gases, but for the PSG films only; the rate for SiO_2 is nearly the same within the period of 0.1 to 10 hours, but the drop from the initial etch rate within the first 6 minutes is greater.

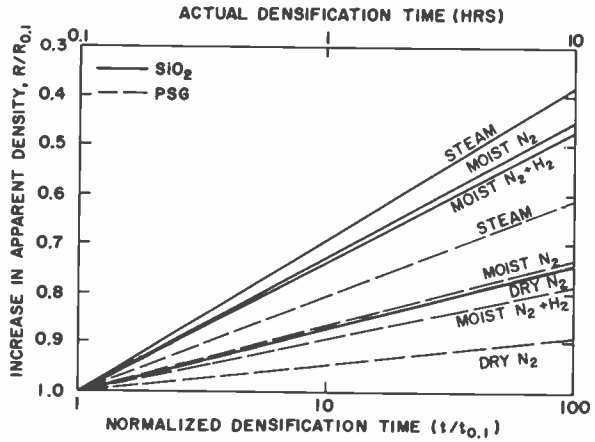


Fig. 3—Increase in apparent glass density of SiO_2 and PSG films as a function of heat treatment time at 450°C in various ambients. Apparent density is represented by the normalized etch rate, $R/R_{0.1}$. Time is normalized at $t/t_{0.1}$. Curves for PSG are average of 2, 3, and 4 wt % P (nominal) stated in Table 2.

Actual and normalized etch rates for the 10 hours of heat treatment are summarized in Table 2 to facilitate numerical comparison between the various treatments for all films. Also listed are actual and normalized values for the rate of densification and the percent decrease in the etch rate. A normalized plot of $R/R_{0.1}$ versus $t/t_{0.1}$ is presented in Fig. 3 for further comparison of the various densification

Table 2—Summary of Results of Low-Temperature Thermal Densification

Parameter	Film Thickness (μm)	Film Composition		Unit	Ambient at 450°C			
		Nominal, wt % P	Exact, wt % P		Dry N_2	Moist N_2	Moist $N_2 + H_2$	Steam
Etch Rate[1] After 10 hours of Densification (P-Etch, 25.0°C)	1.10	0	0	Å/sec	12.6	6.7	7.6	4.4
				Norm[2]	1.00	0.54	0.60	0.35
				% Decr.[3]	26	55	53	62
	1.15	2	2.1	Å/sec	27.3	21.3	21.8	17.7
				Norm	1.00	0.78	0.80	0.65
				% Decr.	8.4	20	19	35
	1.20	3	3.0	Å/sec	33.3	27.2	23.0	22.1
				Norm	1.00	0.82	0.70	0.66
				% Decr.	14	25	33	38
	1.00	4	3.8	Å/sec	(50.7)	(41.5)	35.0	23.0
				Norm.	(1.00)	(0.82)	(0.70)	0.45
				% Decr.	11	20	27	46

[1]Note that etch rate is an inversely proportional measurement of densification (i.e., etch rate decreases as density increases).
[2]All normalized etch rates are normalized to dry N_2 values.
[3]Refers to decrease in etch rate for the densification period of 0.1 to 10 hours.
( )Parenthetical etch rate, normalization, and % decrease values are mathematically derived in proportion to 3% P PSG etch rates.

ambients. The value $R_{0.1}$ corresponds to the etch rate measured after the 0.1 hour ($t_{0.1}$) heat treatment at 450°C. (Initial etch rates taken before the 450°C treatment are subject to some fluctuation due to partial stress anneal and are therefore less accurate.) The slope of the curves between R and $\ln(t)$ illustrates at a glance the relative rate of increase of the apparent glass density under given densification conditions. The plots show that the rate of increase in apparent glass density ($R/R_{0.1}$) is inversely proportional to the logarithm of the heating time. The average lines of the PSG films drawn for a given ambient show a consistently lower rate of densification than do the SiO_2 films.

The effects of thermal densification at 450°C in terms of microcrack formation were examined using glassed IC wafers. Layers of SiO_2 and 2, 3, and 4 wt % phosphorus PSG were deposited on IC device wafers under the usual CVD conditions at 450°C; the layer thicknesses ranged from 1.1 to 1.2 μm. Both linear bipolar IC's (CA3747) with large aluminum-metallized capacitor areas and CMOS IC's (CD4017A) were chosen for these tests. The overcoat layers were delineated by photolithography and chemical etching to open the aluminum bond-pad areas and the grid lines. Microscopic examination of the as-deposited samples showed that the highly stressed SiO_2 layer had cracked along the edges and in the interior of the large aluminum-metallized areas. Additional cracks formed along the entire edge of the circuit over the dense oxide. The glass layers containing 2, 3, or 4 wt % phosphorus exhibited no cracks, thus demonstrating that the incorporation of a relatively small amount of phosphorus into the glass can have a very large effect on preventing glass cracking. These phosphorus-containing samples were then used for densification studies. Heat treatments at 450°C in steam and in a moist H_2-N_2 gas mixture for periods of up to 10 hours were applied. Glassed CMOS device wafers with overcoats of 1.1-μm thickness having $\geq$2 wt % phosphorus showed no signs of crack formation after the 10-hour heat treatment in steam. The linear bipolar IC's with 2 and 3 wt % phosphorus PSG did show some small cracks over the aluminum of the unusually large capacitors, indicating that excessive stresses can form in these extreme cases of large aluminum areas. Moist forming gas (10% H_2 + 90% N_2) was less favorable than steam in preventing crack formation during the extended 450°C heat treatment.

The same IC's described above, which had been specially selected because of their surface sensitivity, were used to assess the effects of densification treatments on electrical properties of test structures. The results are briefly summarized as follows.

(1) In general, positive ion density in the gate oxide of MOS devices increased after 1 hour in wet forming gas at 450°C and after 9

hours in steam at 450°C. The shift in flat-band voltage after bias-temperature stress at 220°C for 5 min was −0.3 to −0.8 V for PSG-passivated gate-metal thermal SiO_2/Si capacitors. Without phosphorus, the shifts were much larger, about −5 V. For the structures tested, a 1-volt shift corresponds to 2.6×10^{11} ions/cm^2. The above data were taken on p-channel MOS transistors where the region under the gate metal has a relatively large perimeter-to-area ratio. For larger-area capacitors over a gate oxide, the shifts after the same temperature-bias treatment were of the order of −20 to −35 V, irrespective of phosphorus content. Before densification, the shift in the C-V curve after bias-temperature treatment was about 0.2 V. These results indicate that positive ions enter the thermal oxide through the metal during densification, and that gettering of the ions occurs by lateral diffusion. Therefore, the small perimeter-to-area capacitors exhibit much larger shifts than those with larger ratios.

(2) Also reflecting increased mobile positive ion density in the oxide was the behavior of lateral p-n-p devices on linear CA3747 wafers. The collector–base and emitter–base avalanche breakdown voltages of these devices showed very large walkout effects after the densification treatments described in (1) above. There was little effect on breakdown voltage of n-p-n devices.

(3) Ten hours of steam at 450°C tended to decrease the leakage currents of both CMOS and linear bipolar devices.

(4) The breakdown voltage of MOS gate oxides was not affected by treatment for 1 hour with wet forming gas. After 9 hours of steam treatment at 450°C, the average gate-oxide breakdown voltage for CVD SiO_2 passivated devices increased from 50 to 62 V, while there was no change in PSG passivated devices.

(5) Threshold voltages of NMOS and PMOS transistors were determined. There were only slight changes (tenths of volts) in the 10^{-6} A threshold voltage, as expected from the results of (1) above.

In summary, there are some changes in electrical properties of test devices after densification treatments. The magnitude of the changes depends upon the conditions of the heat treatments and the particular device type and structure.

4.2 Studies Involving UV Irradiation and Densification in Atomic Hydrogen Plasma

The results obtained in the attempted glass densification at elevated temperature using high-intensity UV radiation as an accelerator were negative. The etch rates, infrared absorption spectra, and metallurgical microscopy indicated that UV irradiation caused no measurable densification or changes in structure or composition of the films.

Results obtained using atomic hydrogen plasma generated by an rf glow discharge as a densifying agent proved partly successful. Etch-rate measurements showed a consistent 20% decrease in the case of the exposed portion of the sensitive 2900-Å-thick SiO_2 films, and a smaller decrease in the thicker SiO_2 films, indicating that a moderate degree of densification can be achieved by this method.

4.3 Film Changes During Storage

We have known for a long time that the infrared absorption spectrum and the chemical etch rate of CVD dielectric films immediately after deposition are different from those measured some time later.[18] The extent of these changes depends on the storage conditions, and reflects effects of ambient sensitive hydration-dehydration reactions accompanied by densification and partial stress release.[7] Infrared measurements of water adsorption on CVD glass films in humid air at room temperature were reported recently.[19]

Etch-rate changes arising from effects of storage must be taken into account in accurate compositional analysis based on etch rate, unless the samples are first densified (800°C) to eliminate these effects by annealing, but often this is not readily possible. The work reported here is the first attempt to systematically examine etch-rate changes of CVD SiO_2 and PSG films synthesized from the hydrides as a function of time under controlled storage conditions.

Results derived from isothermal etch-rate measurements of typical films of CVD SiO_2 and PSG are summarized in Table 3. These results were obtained from data collected over a period of 15 minutes after film deposition to 2500 hours of storage of the films at room temperature in dry air. The plots of the etch rate versus log time were straight lines whose slope represents the rate of densification. The values for the measured etch rate, the normalized etch rate, and the rate of densification stated in Table 3 were read from the curves of best fit through the data coordinates. They show that the rate of densification at room temperature is a logarithmic function of time (as at higher temperature), that the rate of densification is about 6 times greater for SiO_2 than for 4 wt % phosphorus PSG, and that the absolute density increase (in terms of etch-rate decrease) is also greater for SiO_2 than PSG (i.e., 15% versus 8% in 25 hours; 29% versus 18% in 2500 hours).

Analogous analysis of PSG film compositions of phosphorus concentrations intermediate to those given in Table 3 (2 and 3 wt % phosphorus) have shown behavior similar to that of the 4 wt % phosphorus PSG listed. We also found that films deposited under differ-

ent CVD conditions behave differently during storage at room temperature. For example, PSG films of similar phosphorus content, but deposited at greatly different oxygen-to-hydride ratios, exhibited different rates of densification. Some of these effects can be associated with the different rates of film deposition resulting from different O_2-to-(SiH_4 + PH_3) ratios, as explained previously.[11,12,14] Different deposition rates give films of varying density, which in turn exhibit different etch rates.

Table 3—Summary of Results of Long-Term Room-Temperature Densification

Parameter	Film Thickness (μm)	Film Composition (wt % P)	Unit	Storage Time in Dry Ambient (hr) 0.25	2.5	25	250	2500
Etch Rate[1] in P-etch at 25.0°C	0.97	4.1	Å/sec	60.0	55.6	51.3	47.0	42.7
			Norm.[2]	1.00	0.93	0.85	0.78	0.71
			% Decr.[3]	0	7.0	15	22	29
	1.00	0	Å/sec	19.2	18.4	17.6	16.7	15.8
			Norm.	1.0	0.96	0.92	0.87	0.82
			% Decr.	0	4.0	8.0	13	18

[1]Etch rate is an inversely proportional measurement of relative densification, decreasing as density increases. Values are taken from semilog plots of best fit.
[2]Etch rates are normalized to 0.25-hour values.
[3]% Decrease shows exponential decrease of etch rate with time starting with 0.25-hour value.

To study these parameters more closely, the less complicated SiO_2 films were used. The effect of storage in humid laboratory air (~50 to 60% R.H.) on the etch rate has been measured as a function of substrate temperature of deposition and rate of film growth at fixed O_2-to-SiH_4 ratio (18:1). These data are presented in Table 4; both measured and normalized etch rates are shown. The results show that the film deposition rate at 450°C has a pronounced effect on the etch rate, the etch rate increasing with deposition rate. The initial etch rate increases from a low of 21.3 Å/sec for a film deposited at 400 Å/min to 23.3 Å/sec for an intermediate deposition rate of 2000 Å/min, and to 25.2 Å/sec for a film grown at the high rate of 7000 Å/min. All three etch rates decrease linearly with the logarithm of time and at about the same rate, as seen from Fig. 4.

SiO_2 films deposited at the intermediate rate but at lower temperatures (300° and 375°C) had lower initial etch rates than the 450°C film (contrary to what was expected), but the decrease with time was

distinctly slower. It also should be pointed out that the etch rates, both initially and after storage, shown in Table 4 are somewhat higher than those observed for films prepared in subsequent work under similar conditions. This effect may be due to small differences in

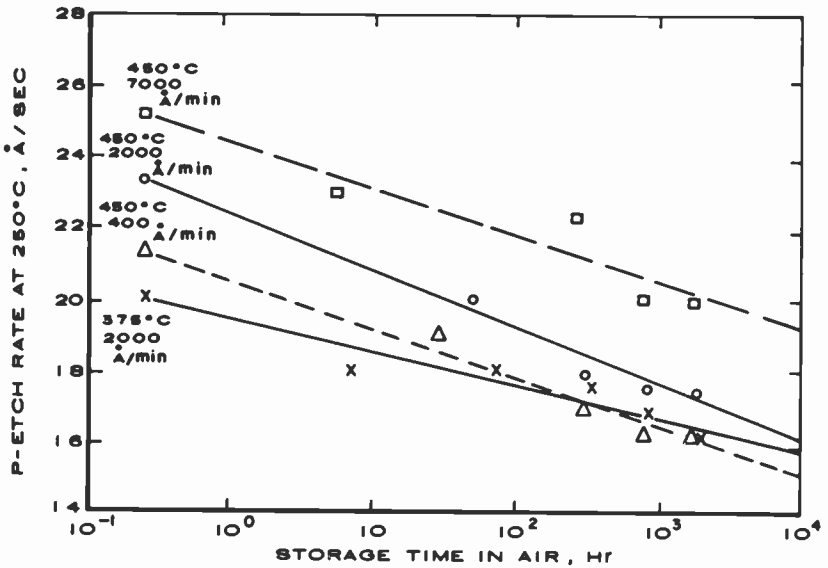


Fig. 4—Etch rate as a function of air storage time of SiO_2 films deposited at 450°C at low, medium and high rates.

CVD conditions that are not fully understood. Nevertheless, the results obtained demonstrate the general behavior and the magnitude and the time-exponential function of the etch-rate decrease with time under room-temperature conditions.

4.4 High-Temperature Densification

As mentioned in the introduction, CVD PSG films on silicon substrate wafers can generally be densified in a few minutes at high temperatures in an inert atmosphere. Examples of the effect of various heating temperatures on the isothermal etch rate of PSG films are shown in Fig. 5. For densification temperatures of 800° and 1000°C, the etch rate decreases very rapidly within the first few minutes of heating, and then decreases slowly and linearly with the logarithm of time. Lower temperatures decrease the etch rate more gradually with time. The effects of such treatments on the chemical etch rate and on the infrared absorption spectrum can be utilized for compositional

Table 4—Etch Rate of SiO_2 Films as a Function of Deposition Temperature, Deposition Rate, and Storage Time

Deposition			Measurement A			Measurement B			Measurement C			Measurement D			Measurement E		
				Etch Rate			Etch Rate			Etch Rate			Etch Rate			Etch Rate	
Run#	Temp. (°C)	Rate (Å/min)	Time (hr)	(Å/sec)	(%)*	Time (hr)	(Å/sec)	(%)*	Time (hr)	(Å/sec)	(%)*	Time (hr)	(Å/sec)	(%)*	Time (hr)	(Å/sec)	(%)*
91-1	300	1500	0.25	22.2	100	—	—	—	243	18.5	83.3	746	18.4	82.9	1776	17.7	79.7
91-2	375	2000	0.25	20.5	100	72	18.0	87.8	337	17.6	85.9	839	16.8	82.0	1867	16.2	79.0
91-3	450	2000	0.25	23.3	100	50	20.0	85.8	314	17.9	76.8	816	17.5	75.1	1844	17.4	74.6
91-4	450	400	0.25	21.3	100	29	19.0	89.2	292	16.9	79.3	794	16.3	76.5	1822	16.2	76.0
91-5	450	7000	0.25	25.2	100	5.5	23.0	91.3	262	22.3	88.5	772	20.1	79.8	1775	20.0	79.4

Fixed CVD Parameters: Reactor: Single-rotation hotplate reactor[12,13]
Total gas flow: 11,050 cm^3/min
O_2/SiH_4 Ratio: 18:1
Film Storage and Analysis: In containers open to laboratory air of ~50 to 60% R.H. at 23°C. Etchant was P-etch[17] at 25.0°C.
See Fig. 4 for *Graphical Presentation of Data*.
* Percent of etch rate at t = 0.25 hr.

film analysis, which is of considerable practical interest and will therefore be briefly discussed.

The etch rate of silicate glasses in suitable etchants is generally a sensitive measure of the chemical composition of the films, and can be utilized as the basis of convenient control tests. We have found that determination of the PSG composition during setting up and optimizing the CVD conditions for a given system is most readily done by the etch-rate method because it is fast, simple, and convenient. It

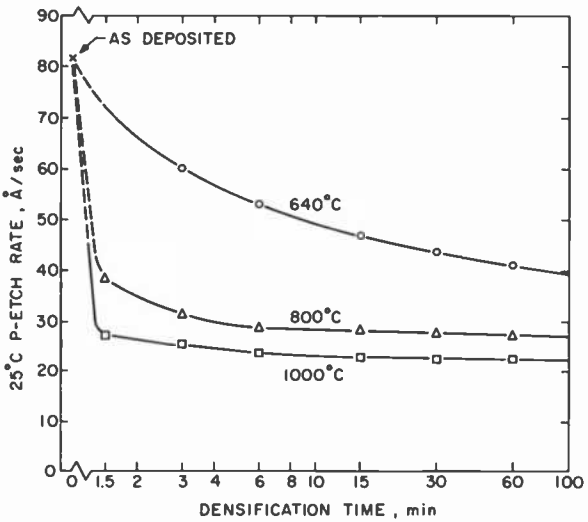


Fig. 5—Etch rate of PSG films (5.1 wt % P) as a function of heat treatment temperature and time in dry nitrogen.

is reliable and sufficiently accurate and precise for most practical requirements if it is carried out under controlled conditions, and if suitable calibration curves are established. However the etch rate is also sensitive, though to a lesser extent, to structural film properties, especially density, porosity, bonding strain, and stress. The effects of these physical film properties can be largely eliminated by a high-temperature annealing treatment at, typically, 800°C. The etch rate then becomes a unique function of the chemical film composition. Therefore, determination of the etch rate of films as-deposited and also after densification furnishes valuable information on both physical and chemical film properties.

The calibration graph presented in Fig. 6 exemplifies the use of etch-rate testing for determining the glass composition. It shows the

etch rate of SiO_2 (0 wt % phosphorus) and PSG films as-deposited under various conditions, and also after densification at 800°C. It can be clearly seen that the etch rate of as-deposited films depends not only on film composition but also on density and stress, which vary with CVD conditions, whereas the etch rate of densified films is a

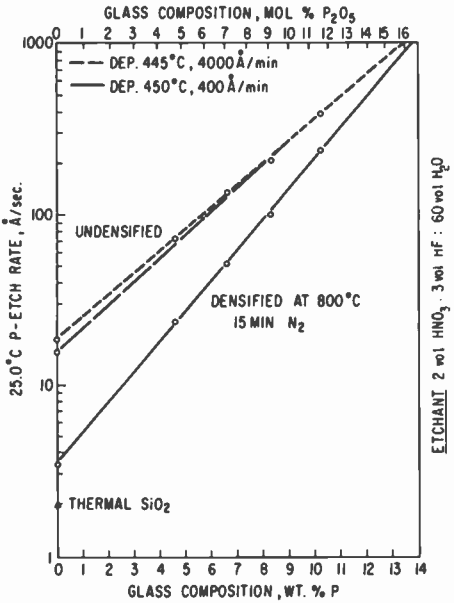


Fig. 6—Etch rates of CVD PSG films as a function of glass composition, deposition conditions, and densification treatment.

unique function of composition. With increasing phosphorus concentration in the PSG, the curves for as-deposited films approach the curve for densified films, indicating that at higher phosphorus concentrations a substantial degree of densification occurs during film deposition. Although curves of different slopes result for films of different density, the logarithm of the etch rate varies in all cases linearly with the wt % phosphorus in the film. Determination of etch rate is carried out as described under film analysis (Sec. 3). Practical applications for IC overcoating analysis have been described in a recent paper.[15]

The infrared absorption spectrum of as-deposited PSG films of low-phosphorus concentration is of rather limited use for quantita-

tive composition analysis. However, the analytical sensitivity can be significantly enhanced by a thermal densification treatment.

The ratio of the intensity of the characteristic P = O vibrational absorbance band at ~1325 cm^{-1} to that of the major Si–O stretching vibration band at ~1050 cm^{-1} is approximately linearly related to the concentration of phosphorus in the glass and can be used with empirical calibration curves of absorbance ratio versus mol % P_2O_5 to estimate the film composition.[20–24] The sensitivity of films as-deposited is not as good as that for the previously published[3,18] analogous methods for B_2O_3, mainly because of the relatively weak absorptivity of P = O. This is a severe shortcoming of the method for application to the analysis of PSG films in the compositional range of main interest (a few percent phosphorus). Previously, we had reported[3] that a densification treatment (typically 15 min at 800°C in N_2) causes spectral shifts in the P = O and Si–O bands, which results in a considerable increase in band resolution. It is now realized that utilization of this effect offers a means of extending substantially the sensitivity and accuracy of the method for measuring P = O absorption in PSG films and, thus, for determining their composition. Furthermore, the densification of samples prior to infrared spectroscopy eliminates the reported[3,23] dependence of the absorbance ratio on deposition temperature, and results in annealing of film stress and bonding strain that are introduced during CVD and that also affect the infrared absorption.

A pair of spectra is presented in Fig. 7 as an illustration. The film was deposited at 371°C, contained 4.5 wt % phosphorus, and was

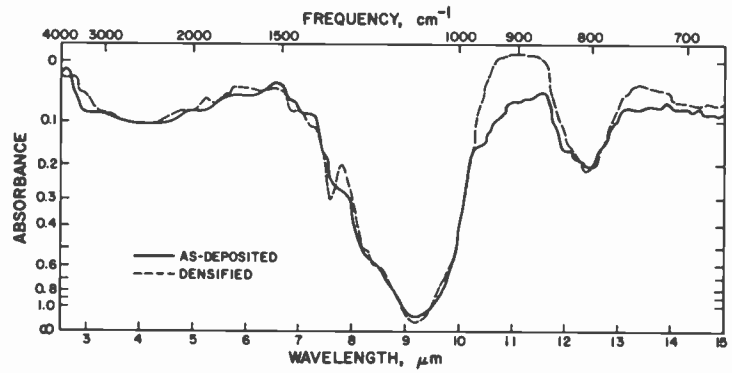


Fig. 7—IR absorption spectra of 4.5 wt % P PSG films before and after densification at 800°C. Note the weak band at about 7.7 μm for the undensified film, and the strong, well resolved band at 7.55 μm, created by the densification treatment of the second film.

14,000-Å thick. Absorbance was measured with a silicon blank wafer in a reference beam of a double-beam spectrophotometer. The spectrum of the film before densification shows only a weak band in the wavelength region of 7.7 μm, only slightly separated from the Si–O major stretching vibration band. In contrast, the same film after densification at 800°C shows a well-resolved band of P = O at 7.57 μm (1321 cm^{-1}).

IR absorption spectra of a relatively high concentration phosphorus glass (7.7 wt % phosphorus) of 19,000-Å thickness deposited at 371°C are shown in Fig. 8. Half of the sample wafer was measured di-

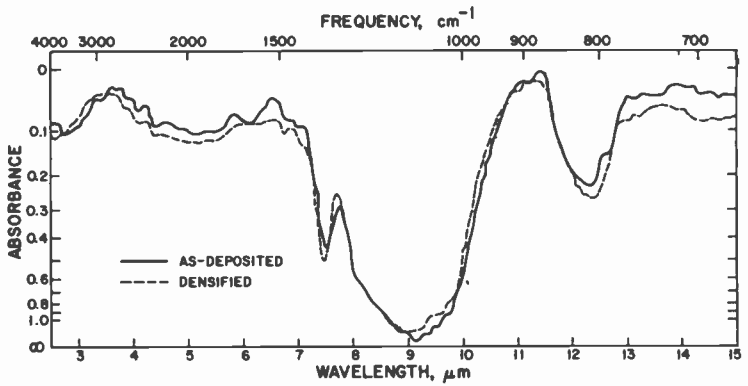


Fig. 8—IR absorption spectra of a 7.7 wt % P PSG film before and after densification at 800°C.

rectly, as deposited, the other half was densified (15 min in N_2 at 800°C). The differences in the P = O band at 7.6 μm are less pronounced than those observed for lower-phosphorus PSG films. Immersion of these samples in boiling water demonstrated resistance of the densified half toward water uptake, in contrast to the undensified sample.[12] This suggests that densification decreases the internal area available for adsorption.

5. Conclusions

(1) CVD PSG and SiO_2 films can be densified to a substantial extent by heating for several hours at 450°C in gaseous ambients containing water vapor as catalyst, as evidenced by isothermal etch-rate measurements. Changes in film properties due to true densification are also evident by infrared spectroscopy and measurements of refractive index and absolute film thickness.

(2) The treatments do not introduce water vapor into the films; in fact, less water tends to be present after densification treatments (even in steam at 450°C) than was initially present after CVD, as confirmed by infrared spectroscopic measurements. Densified films resist water uptake.

(3) No microcracks or other observable defects are introduced in these treatments in typical PSG (but not SiO_2) films of up to at least 1.2-μm thickness, deposited on silicon or over aluminum-metallized linear bipolar or CMOS IC's, as shown by microscopic examination and selective aluminum etching.

(4) Electrical measurements (channel leakage, interelectrode and junction currents; breakdown and MOS threshold voltages; capacitance-voltage with bias-temperature stress) indicate that some of the electrical properties of linear bipolar and CMOS test devices glassed with PSG overcoatings are affected to a certain degree by the steam or moist-gas heating treatment at 450°C for periods of up to 10 hours.

(5) No densification effects were detectable in SiO_2 and PSG films on exposure to high-intensity ultraviolet radiation in room air at elevated temperature.

(6) Exposure to atomic hydrogen plasma at elevated temperature in low-pressure H_2-Ar led to a moderate degree of densification in the more sensitive SiO_2 films.

(7) Room-temperature storage of SiO_2 and PSG films in dry or humid air leads to an etch rate decrease due to densification and stress release effects. Measurements taken at intervals of from 15 minutes after CVD to over a thousand hours of storage have demonstrated that the etch rate decreases linearly with the logarithm of time, analogous to the effects observed at higher temperatures. In all cases, the rate and absolute level of decrease depend on the phosphorus content of the films, the CVD conditions, and the densification conditions.

(8) High-temperature treatments (800°C, N_2) for a short period of time (10 minutes) of PSG and SiO_2 films cause their etch rates to decrease very rapidly (1.5 min) to a level lower than obtainable at 450°C in steam for many hours. Beyond this period of heat treatment, the etch rate decreases linearly with the log of time at a very low rate. The degree of densification attained by this heat treatment diminishes as the phosphorus concentration increases. The largest degree of densification results at 0 wt % phosphorus (pure SiO_2), namely, about 4-fold in terms of etch rate. The two curves (See Fig. 6), converge at about 15 wt % phosphorus (17 mol % P_2O_5), indicating

no additional densification on heating films of this and higher phosphorus content. The high phosphorus content apparently yields a high-density film as-deposited at 450°C.

(9) Application of high-temperature densification is of great practical importance in analytical work and has been utilized for monitoring the film composition.[11,12,14,15].

(10) A short high-temperature densification at 800°C (or extended heating at 450°C) of PSG films has been demonstrated to be a useful technique in analytical infrared absorption spectroscopy, enhancing the resolution of the P = O vibrational band and substantially improving the sensitivity of the infrared method for determining low concentrations of phosphorus in PSG films.

Acknowledgments

I would like to express my thanks and appreciation to R. B. Comizzoli for contributing data on electrical measurements, to C. E. Tracy for carrying out the irradiation experiments, to R. D. Vibronek for performing the etch-rate measurements, to B. Goydish and J. Sabo for wet chemical analyses, and to J. M. Shaw for ellipsometry. I wish to thank also G. L. Schnable and N. Goldsmith for critically reviewing the manuscript.

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Analysis of Glass Passivation Layers on Integrated-Circuit Pellets by Precision Etching*

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Abstract—A new microanalytical method has been devised for determining the structural defect density, layer structure, layer type, and chemical composition of glass passivation overcoat layers on single pellets of aluminum-metallized IC devices, including hermetically packaged and plastic encapsulated types. The method is based on selective chemical etching. Localized structural defects are determined by application of an aluminum etchant. Layer structure and composition are determined by isothermal quantitative glass etching combined with film thickness measurements on a microscale. It is shown that isothermal etch rate measurement of SiO_2-PSG passivation layers is a reliable, fast, and convenient tool for determining film composition of both simple films on silicon and of complex film structures. Generally applicable calibration graphs have been established and experimentally demonstrated.

Two techniques of the method were developed. One is based on graphical resolution of layer thickness versus etch time plots, and the other on step etching combined with profilometry. The validity and usefulness of the new techniques have been demonstrated experimentally by application to comparative evaluation of commercial linear bipolar and MOS IC's from various manufacturers. The results obtained from this comparative survey have served to assess the type and quality of IC glass passivation in industry in the recent past and at present.

1. Introduction

Integrated circuits that are packaged by plastic encapsulation techniques require a protective and passivating dielectric overcoat to

* This work was in part supported by the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-74-C-5146.

maintain electrical stability, to prevent mechanical damage, and to assure device reliability.[1] Layers of oxide or silicate glasses prepared by chemical vapor deposition (CVD) are most commonly used for this purpose.[1-3]

It is frequently necessary to assess the quality of passivating glass overcoats on both MOS and planar bipolar types of IC pellets for the purpose of in-house quality control, reliability testing, or evaluation of competitors' products. In most cases, the glass overcoat consists of vitreous silicon dioxide (SiO_2), phosphosilicate glass (PSG), or a combination of these layers over aluminum-metallized IC's. If the devices are encapsulated in epoxy molding compounds, exposure of the pellet without damage is required before analysis can be made. If the devices are contained in a hermetic enclosure, their exposure is readily accomplished by mechanically opening the container.

Three factors must usually be determined:

(1) integrity of the glass layer (pinhole density, microcracks, blisters, and other localized defects);
(2) layer structure (type, sequence, and thickness of the layers making up the glass coating);
(3) chemical composition of each layer.

From the results, the quality of the glass overcoating can be assessed and the processing sequence inferred.

Several methods were tested for suitability to microanalytical applications for determining the structure and composition of overcoating layers on single IC pellets. Instrumental x-ray fluorescence analysis or surface resistivity measurements after high-temperature diffusion for determining the phosphorus content in PSG films,[1,3] although excellent methods for larger samples, are not applicable in this case. Instrumental composition-profiling microprobe techniques,[4] particularly those based on electron-probe microanalysis,[5] Auger electron spectrometry,[6,7] and MeV ion backscattering spectrometry,[7] are certainly the methods of choice from a purely analytical research point of view, but these sophisticated methods are far too complicated for routine use in a control laboratory of a manufacturing facility when large numbers of samples must be analyzed rapidly. After exploratory work on quantizing electron-probe micro-analytical techniques and scanning Auger electron spectrometry, we decided to devise a simple but reliable method based on etch-rate analysis using the principles discussed in the next section. When combined with aluminum marker-etching techniques,[8] this method can be used to determine the chemical composition, the component layer structure, the component thicknesses, the integrity of the dielectric overcoating,

and the density of localized structural defects over aluminum metallization. Furthermore, the thickness of the dense SiO_2 layer underneath the aluminum can be readily determined at the same time without extra effort.

Two etch-rate techniques have been developed for performing the analysis. The first ("standard technique") is applicable to the analysis of practically all types of SiO_2/PSG overcoating structures and is very accurate and reliable, but it requires a number of data points to establish a graph of etch time versus overcoating thickness from which the component thicknesses and compositions are determined. The second ("simplified technique") is faster in that it requires only total-etch-time measurement and one or two contour measurements using a stylus instrument such as a Talysurf.* However, it works only if definition of the layer contour is sufficiently sharp for graphical resolution, which is not always the case. Both techniques are presented in detail and compared experimentally. The basis of quantitative chemical etching is discussed first since it underlies both techniques.

2. Chemical-Etch-Rate Measurements for Composition Analysis of Glass Films

The main purpose of this section is to examine the general principles and techniques of etch-rate analysis. These are directly applicable for analyzing uniform oxide and glass films on semiconductor wafer pieces of a few square centimeters or less. Applications to IC pellet analysis are treated in subsequent sections.

The etch rate of silicate glasses in suitable etchants is generally a sensitive measure of the chemical composition of the film and can be utilized as the basis of convenient control tests. We have found, for example, that determination of PSG composition is most readily done by the etch-rate method, because it is fast, simple, and convenient.[2] Once suitable calibration curves are established, it is reliable and sufficiently accurate and precise for most practical requirements.

The etch rate method is also sensitive, though to a lesser extent, to structural film properties, especially density, porosity, bonding strain, and stress, rendering it valuable in process control for monitoring these film properties. The effects of these physical film properties can be largely eliminated by a high-temperature annealing (densification) treatment at, typically, 800°C. The etch rate then becomes a unique function of the chemical film composition.

Determination of the etch rate of films as deposited and after

* Taylor-Hobson, Ltd., England.

densification can therefore furnish information on both physical and chemical film properties. The calibration graph presented in Fig. 1 exemplifies the use of etch rate testing for determining the glass composition. It shows the etch rate of SiO_2 (0 wt % phosphorus) and PSG films as deposited under various conditions, and also after densification at 800°C. It is clear from Fig. 1 that the etch rate of as deposited films depends not only on film composition but also on density and stress, which vary with CVD conditions, whereas the etch rate of densified films is a unique function of composition. Higher densification temperatures, such as 900° and 1000°C, cause some additional decrease in the etch rate of the films with low phosphorus content.[23]

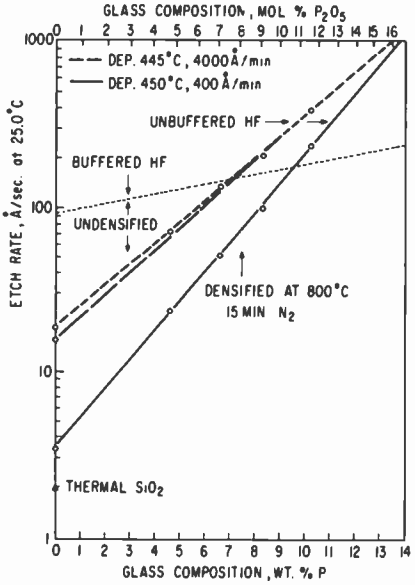


Fig. 1—Etch rate of CVD PSG films as a function of glass composition, deposition conditions, densification treatment, and etchant composition (as defined in Table 1).

With increasing phosphorus concentration in the PSG, the etch rate curves for as-deposited films approach those for densified films, indicating that at higher phosphorus concentrations, a substantial degree of densification occurs during film deposition. Although curves of different slopes result for films of different density, the logarithm of the etch rate varies in all cases linearly with the wt % phosphorus in the film. Details on the CVD aspects[2,3] and parameters of film densification[23] have been presented elsewhere.[2,3]

Table 1—Selectivity of Chemical Etch Rates for CVD SiO_2 and PSG Films[1]

Etchant Composition	Etch Rate (Å/Sec) at 25.0°C				Etch Rate Ratio[2] (12% PSG/SiO_2)	Comments
	SiO_2	3.3 wt % P PSG	9.0 wt % P PSG	12 wt % P PSG		
A. 1 vol HF 49% 4 vol H_2O	86.9	231	1040	4000	46	Good selectivity but etching too fast
B. 3 vol HF 49% 60 vol H_2O 2 vol HNO_3 70%[3]	15.9	45.6	281	706	44	Good selectivity and etching at convenient rates
C. 3 vol HF 49% 62 vol H_2O	18.8	39.8	260	619	33	Somewhat lower selectivity and lower etch rates than B
D. 453.6 g (1 lb) HF 49%, 2608 g (5.75 lb) NH_4F 40%, 1400 ml CH_3CO_2H 99.3%	119	155	254	324	2.7	Extremely low selectivity; useless for analytical purposes but excellent for pattern etching
E. 453.6 g (1 lb) HF 49%, 2608 g (5.75 lb) NH_4F 40%	91.5	116	160	213	2.3	Similar to D, with still lower selectivity and lower etch rates

[1] Films deposited from $SiH_4 + N_2 + O_2 \pm PH_3$ at 450°C as described in Refs. [2] and [3].
[2] This ratio was chosen arbitrarily as a measure of the relative etching selectivity.
[3] "P-Etch"[10]

Primary calibration of phosphorus concentration in PSG for all our analytical work was based on wet chemical colorimetric analysis utilizing ammonium molyhdate reagent. For this purpose the films were first dissolved in HF solution followed by elimination of all dissolved silicon to prevent its interference in the molybdate reaction. Two or three colorimetric tests were made per sample to obtain an average value.

Determination of etch rate is carried out by measuring the film thickness and by measuring the dissolution time in the etch solution under isothermal conditions. Direct interferometric techniques of thickness measurement can be employed (see, for example, Ref. [9]) if the refractive index of the film is known. Multiple-beam interferometry of metal-coated samples yields the thickness independent of refractive index. For single films, ellipsometry can be used; it yields both thickness and refractive index of the film. One of the simplest absolute techniques is profilometry of a step etched down to the substrate, as described in Section 5.2.

Diluted HF solutions can be used as etchants. We found an etch temperature of 25° ± 0.2°C and a mixture of 2 vol HNO_3 (70%), 3 vol HF (49%), and 60 vol H_2O (P-etch)[10] convenient for CVD films of typically 1-μm thickness. This mixture is slightly more selective for PSG composition than water-diluted HF solutions. Ammonium-fluoride-buffered HF solutions should not be used because their selectivity for phosphorus in PSG films is extremely poor; the sensitivity of dilute HF solutions is considerably greater. A comparison of etch rates in various etchant compositions is given in Table 1. Etching is performed either integrally until the entire film is dissolved, or differentially until a desired portion is etched off. In the first case, the hydrophobic property of the substrate can be used as an end point if the substrate is silicon. In the second case, an additional thickness measurement is required to obtain the residual and incremental film thicknesses. Details of the technique, including the use of a convenient etch apparatus for automatic sample movement, were described in a previous publication.[11]

It is frequently necessary, in PSG evaluation and comparison with literature data, to convert etch-rate results obtained by other methods from weight-percent phosphorus to mole-percent phosphorus pentoxide. A conversion graph for this purpose is shown in Fig. 2.

It is often convenient to relate the etch rate of a PSG film directly to the silane/phosphine ratio used in the CVD of the film. A plot of data for this application is presented in Fig. 3; the same samples and CVD conditions as in Fig. 1 were used to construct this plot. Also shown for comparison are etch rates for various types of SiO_2 films.

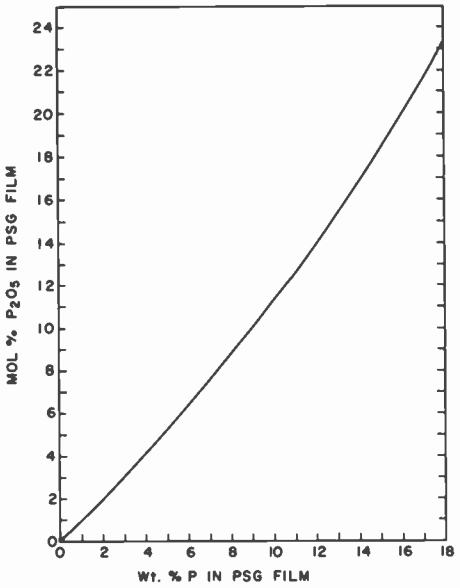


Fig. 2—Correlation of mol % P_2O_5 and wt % phosphorus in PSG films.

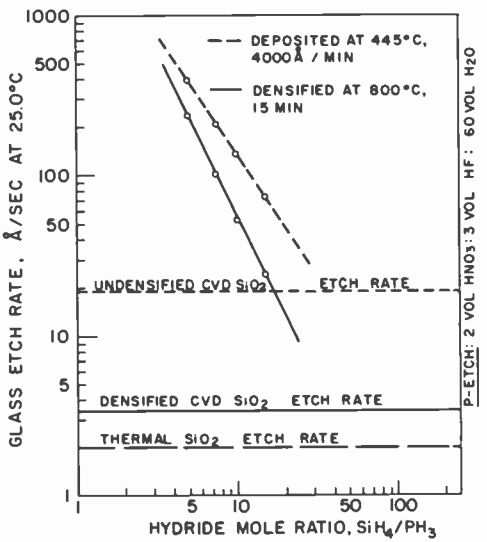


Fig. 3—Etch rate of PSG films versus silane/phosphine ratio in the hydride gas mixture. Etch rates for as-deposited, densified, and thermally grown SiO_2 films are shown for comparison.

This type of calibration curve is particularly useful for setting up CVD conditions and for estimating the hydride gas ratio that had been used to prepare a given PSG film at a known substrate temperature of deposition.

The general principle of etch-rate analysis can also be applied for characterizing films other than silicate glasses, such as plasma-deposited silicon nitride overcoatings on IC's, as will be demonstrated. Furthermore, the etch-rate method is useful in more complex analytical applications where composite films must be resolved into their com-

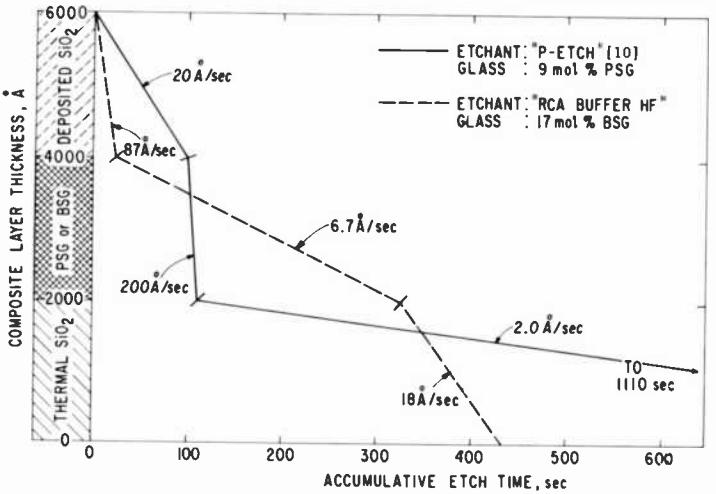


Fig. 4—Application of selective etch method for analyzing multilayer dielectric structures.

ponents.[9,10,12] It is possible to identify composition and thickness of film layers in multilayer structures by plotting composite film thickness versus time of etching. A schematic plot of two hypothetical cases of triple film structures is presented in Fig. 4 to illustrate the technique. Practical applications of this technique for IC overcoating analysis are described in the subsequent sections.

3. Preparation of IC Pellet for Analysis

IC's that have been diced into pellets and have not undergone mounting are best positioned on a piece of silicon scrap wafer to facilitate handling (glass substrates are not suitable). Several pellets are mounted with a melted adhesive resin or with double-sticking adhesive tape. No further preparation is needed.

In most cases the device to be analyzed is either hermetically packaged or plastic encapsulated, requiring exposure of the pellet. Hermetically packaged units in metal cans or ceramic packages are readily opened by simply removing the lid mechanically. Plastic-encapsulated units require mechanical and chemical partial decapsulation.

Commonly used plastic encapsulants consist of formulations based on bisphenol A epoxy, epoxy–novolac, silicone, or phenolic resins filled with a high percentage of mineral powders such as silica and alumina, and chopped glass fibers. A few techniques for removal of encapsulants have been described in the literature.[13,14] In some instances extended treatments in hot N,N-dimethylacetamide for certain epoxies, or in hot 1,1,3,3-tetramethyl-guanidine[15] for silicone molding compounds can be used. The decapsulation techniques that we have found to be particularly effective for many different types of encapsulants are described in Appendix 1. An example of a decapsulated IC is shown in Fig. 5.

After decapsulation and before analysis, the pellet is examined under a microscope for device geometry, surface cleanliness, and gross defects such as cracks and blisters in the overcoating and severe damage to the aluminum interconnects. Particulate impurities that may have remained from the decapsulation treatment are removed by gentle swabbing of the pellet with a Q-tip soaked in trichloroethylene, followed by rinsing with a jet of the same solvent and blowing dry.

4. Standard Analysis Technique

First, we will describe the full analysis technique developed as a standard. A simplified and faster, but less accurate, version of this technique is then described in Section 5.

4.1 Dielectric Integrity Testing and Removal of Bond Wires

The package with the exposed, cleaned pellet is immersed in aluminum etch [40 vol H_3PO_4 (85%):10 vol H_2O:4 vol HNO_3 (70%)] at an etchant temperature of 50°–55°C for twice the time required to dissolve the aluminum in the bonding pads.[8] This is followed by water rinse, blowing dry, and microscopic inspection for pinholes, microcracks, and other defects in the glass layer over the aluminum. The type and frequency of defects are recorded.

After the integrity testing is completed, the bond wires are pulled off the IC bonding pads with tweezers under a binocular stereomi-

croscope. This is readily accomplished, and is necessary in most cases to allow later observation of the pellet at 500× magnification.

4.2 Preparation of Dielectric Taper

Next, the aluminum-etched pellet is placed under a binocular stereomicroscope and partially masked with wax. We use a viscous solution

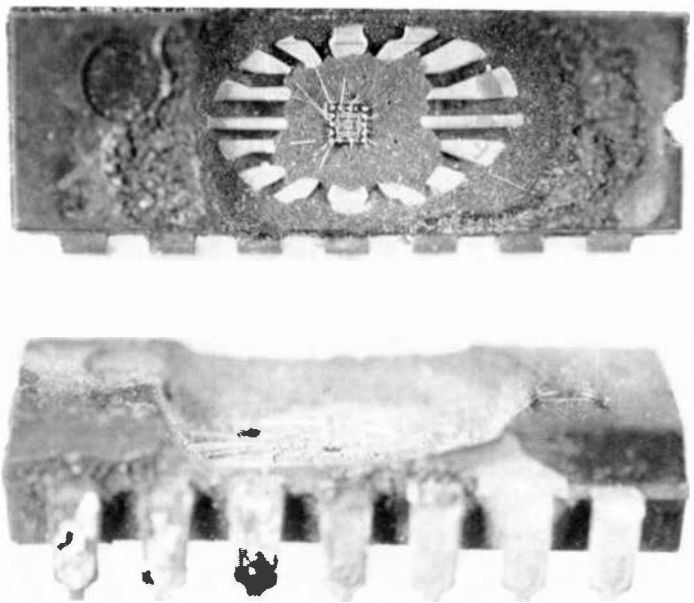
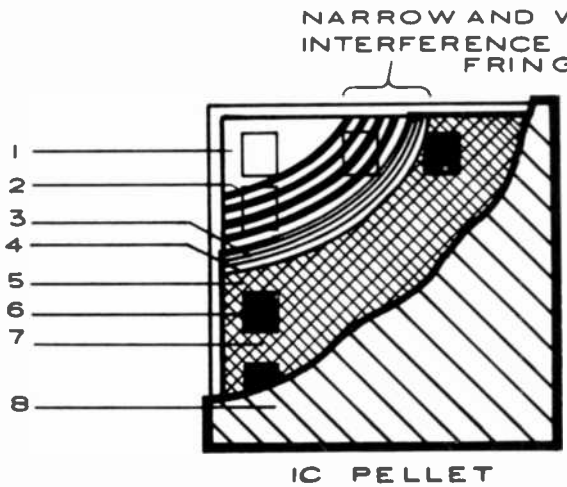


Fig. 5—Top and side views of a partially decapsulated IC ready for pellet analysis. Length of epoxy molded package is 18 mm.

of Apiezon Hard Wax W* in trichloroethylene and apply it with a fine-tipped sable paint brush. About 90% of the pellet is covered with a thick layer leaving only one corner exposed, as shown in Fig. 6. The sample is then placed on a warm hotplate just long enough to melt the wax.

* J. G. Biddle Co., Plymouth Meeting, Pa. 19462.

The sample is cautiously immersed in concentrated HF (49%) at room temperature to etch off both overcoat and dense SiO_2 layers down to the silicon substrate. It usually takes from 30 to 60 seconds to strip these layers, depending on their thicknesses and composition. The endpoint is readily detected by examining the water-rinsed sample under the microscope in white light. All interference colors will



Legend:
1. Area stripped of glass (Si substrate)
2. Etched dense SiO_2 bottom layer taper (wide)
3. Etched PSG taper (narrow)
4. Etched SiO_2 top layer taper (wide)
5. Area for etch-rate determination (preferred)
6. Bonding pad oxide area for precision etching
7. Original glassed area
8. Second masking for precision etching

Fig. 6—Schematic of taper-etched IC pellet prepared for precision etching.

have disappeared when the silicon is fully exposed, and the surface is hydrophobic. Excessive overetching must be avoided because it will narrow the taper of the overcoat, rendering the subsequent measurements more difficult. It is therefore best to etch initially for 30 seconds and then to completion in 10-second steps.

Finally, the wax mask is completely removed in warm trichloroethylene baths and a new coating of wax is applied so that the area with the etched taper is fully exposed (Fig. 6). The masked portion of the pellet is reserved for a possible repeat analysis. Photomicrographs of typical tapers on IC's formed by HF-etching are shown in Figs. 7 and

8. A schematic cross-section of the resulting taper contour is presented in Fig. 9.

4.3 Precision Etching of Overcoat Layers

(a) We can now measure the thicknesses of the SiO_2 layer and overcoat layer by using the taper formed down to the silicon. An unob-

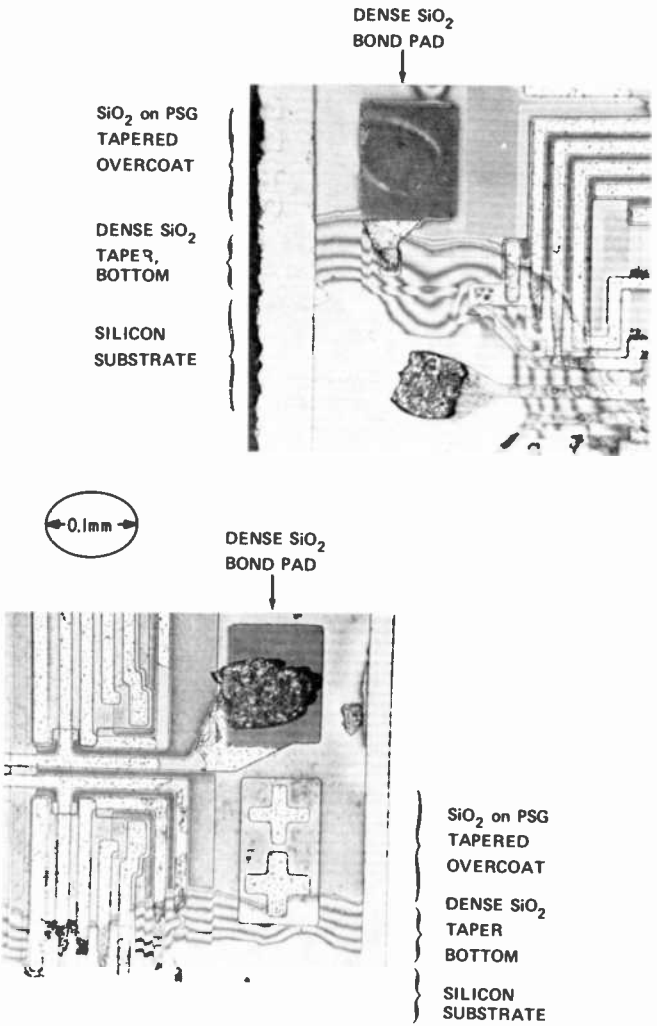


Fig. 7—Photomicrographs of interference fringes in monochromatic light from typical oxide and glass tapers on IC's prepared for precision etching.

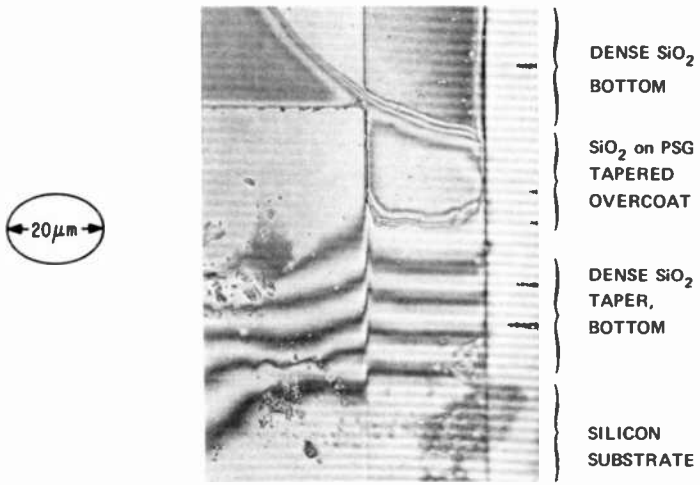


Fig. 8—Photomicrograph of interference fringes on monochromatic light from typical oxide and glass tapers on IC's prepared for precision etching.

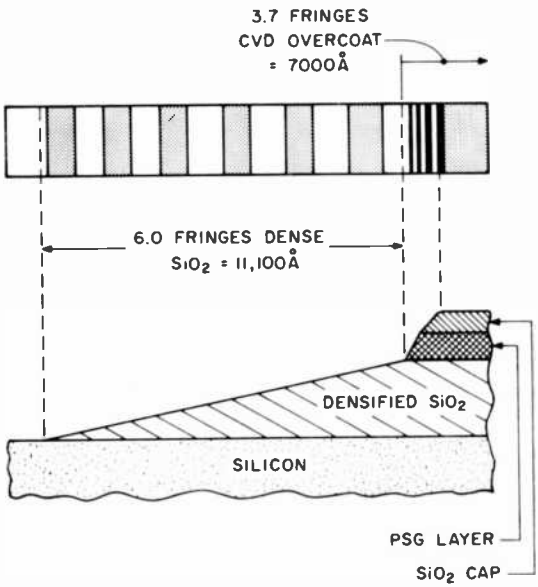


Fig. 9—HF-etched dense oxide and overcoat layer structure of a typical IC. The top figure shows interference fringes of the taper contour shown below, as seen perpendicular to the surface in monochromatic light. The bottom figure is a schematic cross section of taper contour (vertical dimensions to scale; horizontal dimension compressed approximately 15 times).

structed, clear area of a well-defined taper portion near one of the pellet edges (preferably between bonding pads) is selected and used for this and all subsequent measurements. A simple method requiring only a good microscope and a monochromatic light source is interference fringe counting. The number of complete and partial dark contour fringes of the dielectric layer taper are counted, including those at the top surface of the taper. This can be done quickly after brief training; a magnification of 500× is usually necessary for adequate resolution. It is important to count any partial top fringe (separated from the last complete fringe by a light fringe) by estimating the shade of darkness. A good description of the technique of fringe reading has been given by Booker and Benjamin.[16] As shown in Fig. 9, the widely spaced and broad dark fringes beginning at the silicon surface represent the dense SiO_2 layer under the metallization. The narrow fringes terminating in the top surface represent the faster etching overcoat layer or layers.

(b) The device is placed under a microscope with perpendicular white light and the interference color of the oxide in the bonding pad areas, where the aluminum was etched away, is carefully noted. These areas are usually thermal or densified SiO_2 and will serve as a check in step (d) below.

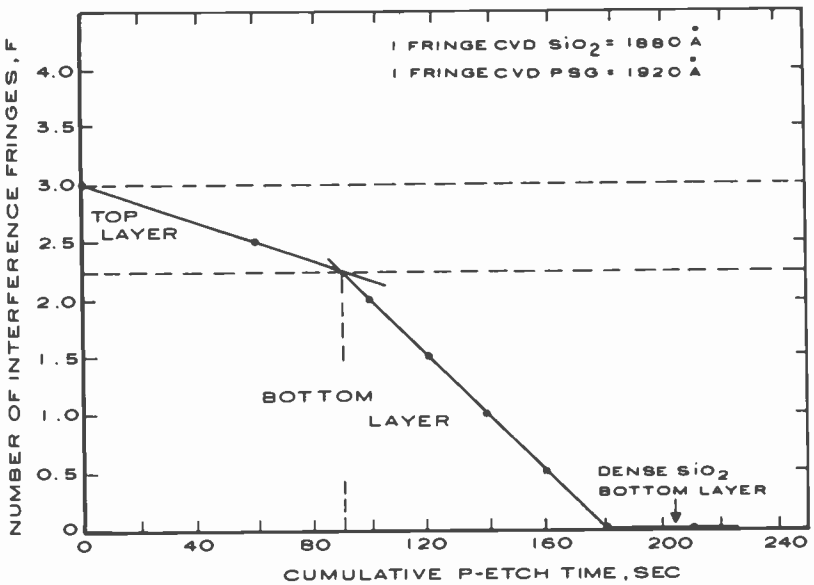
(c) The remasked device is then immersed in P-etch [13 vol HF (49%), 60 vol H_2O, and 2 vol HNO_3 (70%)] maintained at 25°C (constant temperature bath) for 60 seconds, rinsed and blown dry. The narrow fringes of the etched glass top layer are remeasured.

(d) Step (c) is repeated several times, but using shorter etch periods of 20 seconds, as seen in the example in Fig. 10. This process continues until the glass is completely removed and the oxide interference color in white light is now the same as was noted under the bonding pads before glass etching. Additional verification of the endpoint is the beginning of dissolution of the aluminum interconnections as they become exposed. Continued etching in P-etch decreases the residual SiO_2 thickness very slowly because of its low etch rate (see Fig. 3).

4.4 Determination of Layer Thicknesses, Layer Types, and PSG Composition

We can now plot the fringe counts versus etch time and draw straight lines of best fit through the points, as shown in Fig. 10, which is an example of an actual analysis of an IC overcoat. Two lines of different slope indicate the presence of two different layers, such as SiO_2 over PSG.

The net thickness and net etch time of each layer is determined from the intercept, and the etch rates (Å/sec) are calculated as shown in the example in Fig. 10. The number of fringes r is related to film thickness d by the well-known relationship, $d = r\lambda/2n$, where n is the



Example of Calculations:

	Top Layer	Bottom Layer
Net Fringes	3.0 F-2.25 F = 0.75 F	2.25 F-0 F = 2.25 F
Thickness	0.75 F × 1880 Å/F = 1410 Å	2.25 F × 1920 Å/F = 4300 Å
Net Etch Time	90 sec	180 sec − 90 sec = 90 sec
Etch Rate	1410 Å/90 sec = 16 Å/sec	4300 Å/90 sec = 48 Å/sec
Layer Type	undensified SiO_2	CVD PSG (undensified)
Composition		3.3 wt % P (from calibration curve)

Fig. 10—Example of a determination of layer thickness, type, and composition from etching and fringe count data.

refractive index of the layer and λ is the wavelength of the monochromatic light used. The wavelength of filtered mercury green light is 5461 Å; that of filtered sodium yellow light is 5890 Å. Undensified CVD SiO_2 has a refractive index of typically 1.45, PSG one of typically 1.42. For mercury light, one contour fringe therefore corresponds to approximately 1880-Å SiO_2 or to 1920-Å PSG; for sodium light the values are 2030-Å SiO_2 and 2070-Å PSG per fringe.

The thickness of the thermally-grown or densified CVD SiO_2 layer underneath the overcoat (and underneath the aluminum interconnection lines) can be readily determined from the fringe count by using a refractive index value of 1.48.

The calibration curve for undensified PSG presented in Fig. 1 is then used to relate the PSG glass etch rate to the phosphorus concentration in terms of wt % P. As already noted, the relation to the CVD hydride composition can be estimated from Fig. 3; however, the substrate temperature of deposition must be known, since the phosphorus content in PSG decreases with increasing deposition temperature.[2,3]

4.5 Repeat Analysis and Evaluation of Multiple Layers

A repeat of the precision etching of the overcoat layers may be desirable in some cases where the taper of the overcoatings produced by the HF 49% etching, is not sufficiently gradual to permit adequate optical resolution. The new taper formed in the overcoat layers during the precision etching is usually more gradual because of the slower etch rate. The steps outlined in Sections 4.2, 4.3, and 4.4 are repeated to obtain a second set of data.

The analyses of multiple layer structures based on SiO_2 and PSG, such as overcoatings of SiO_2/PSG/SiO_2 over aluminum metallization evaporated on CVD SiO_2 deposited on thermally grown SiO_2, are performed by the same techniques. The relative density of the SiO_2 layer on silicon can be estimated from the etch-rate measurement if the etching is continued down to the silicon substrate. Several examples of actual IC analyses graphs showing a variety of layer structures are presented in Fig. 11.

4.6 Precision and Accuracy

The precision and accuracy depend primarily on the film thickness, the quality of the taper contour, the reading of the interference contour fringes, and the reliability of the % P calibration curve. The routine accuracy of a single contour fringe measurement is within ±350 Å;[16] for a typical overcoating thickness of 5000 Å this would correspond to ±7.0%. However, since several measurements are taken for graphical resolution, the accuracy of the thickness values in our case is much better. The precision of the calibration curve for phosphorus is better than ±5%; the absolute accuracy is estimated to be within ±10%.

A less significant second-order error is introduced when undensi-

fied samples are analyzed by the techniques described so far, since the etch rate of the undensified films is influenced to some extent by the CVD conditions used to prepare the overcoat layers. More accurate values of the phosphorus content can be obtained if the passivation glass is densified and the calibration curve for densified SiO_2 and PSG is used. To achieve this, the isolated device pellet is heat-treated at 800°C in nitrogen for 15 minutes before the precision etch analysis is performed. The corresponding calibration curve in Fig. 1 for densified layers is then used to determine the composition.

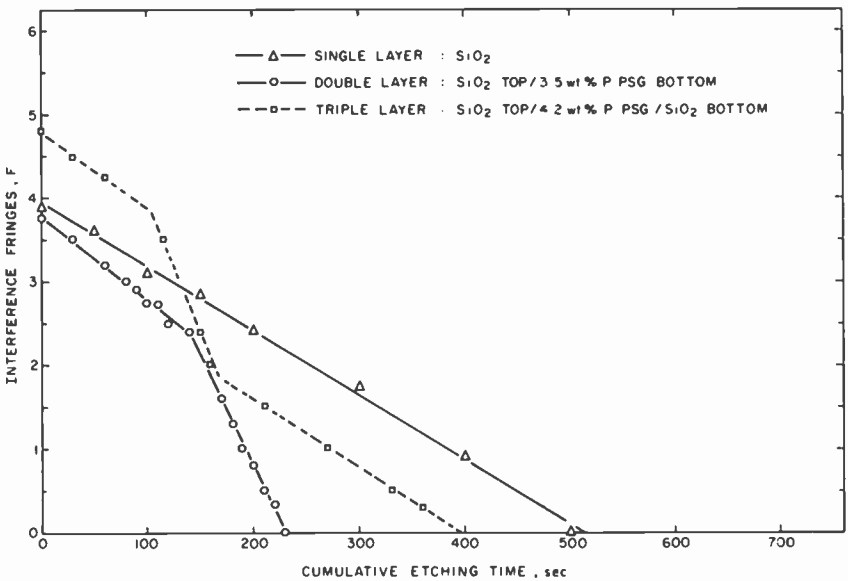


Fig. 11—Example from actual IC analyses of typical etch time versus film-thickness interference fringes measured for various types of layer structure: single, double, and triple layers.

5. Simplified Analysis Technique

As in the standard technique, the device pellet is prepared for analysis as described in Appendix 1 and is processed through dielectric integrity testing (4.1) and taper etching (4.2). The simplification in the procedure begins at this point. The rather tedious interferometric thickness measurements are eliminated; etching is continued until the exposed overcoating has been removed; and the layer thicknesses

are then determined from a stylus trace recording. The details are as follows.

5.1 Determination of Etching Time of Overcoat Layers

First, we examine the initial oxide pad interference color as noted in Section 4.3 (b). The sample is etched in P-etch as described in Sections 4.3 (c) and 4.3 (d), but using the oxide interference color instead of fringe measurement to determine the endpoint. Total etch time required to remove the overcoat layers is noted. The wax mask is then dissolved in warm trichloroethylene baths.

5.2 Profilometric Measurements

A surface profilometric trace recording is obtained across the etched steps (20,000× vertical and at least 100× horizontal magnification) using a stylus instrument.* It is best to position the stylus in the area between the bond pads and the edge of the delineated IC pattern. The trace is repeated on the opposite side of the pellet. A good description of stylus measuring techniques and principles has been recently published.[17]

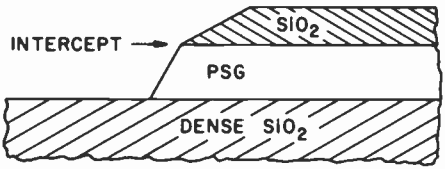


Fig. 12—Schematic cross section of a typical CVD overcoat double layer after step etching for profilometry.

The thickness of the dense SiO_2 bottom layer (under the aluminum metallization) can then be read directly from the step formed in the 49% HF etch down to the silicon surface. The thickness of each overcoat component layer can also be obtained from the trace recording, using the intercept or intercepts of the curves, as shown schematically in Fig. 12 for a SiO_2 on PSG double layer.

* For example: Talysurf by Taylor-Hobson, Ltd., England; Dektak by Sloan Instruments Div., Santa Barbara, Calif.; Micro-Topographer 200 by Gould, Inc., Measurement Systems Div., El Monte, Calif.; and Proficorder by Bendix Industrial Metrology Div., Ann Arbor, Mich.

5.3 Calculation of Layer Compositions

We can now calculate the PSG etch rate R_{PSG} from the following equation:

$$R_{PSG} = \frac{D_{PSG}}{t - (D_{SiO_2}/R_{SiO_2})},$$

where

R = etch rate (Å/sec),
D = film thickness, (Å),
t = total etch time (sec),
SiO_2 = silane oxide top layer
PSG = phosphosilicate glass layer, and
R_{SiO_2} = 16 Å/sec for as-deposited SiO_2 (IC pellet not heat treated), 3.4 Å/sec for SiO_2 films densified at 800°C (15 min N_2).

The calculated value of R_{PSG} is then used to read off wt % phosphorus from the calibration curves for the undensified or densified PSG (Å/sec versus wt % P), depending on whether or not the pellet was heat treated.

5.4 Comparison of Simplified and Standard Techniques

The precision and accuracy of the simplified technique depend primarily on the quality of resolution of the step trace thickness values. The results of repeatability tests of profilometric thickness measurements of typical PSG/SiO_2 double layers are presented in Table 2. These data indicate that the variations for single films are generally within ±10%. The total thicknesses listed were also measured by contour fringe interferometry. The values were within 3% of those obtained by Talysurf averaged measurements. Reproductions of three actual typical Talysurf step-traces are shown in Fig. 13 as examples. The precision and accuracy of the phosphorus calibration curves are the same as noted in Section 4.6.

The results of a comparison between the two techniques using PSG/SiO_2 layer structures on silicon substrate wafers are presented in Table 3. Results comparing the techniques in actual IC analysis are given in Table 4.

The Talysurf profiles at 20,000× vertical and 100× horizontal magnifications are usually adequate for resolving typical PSG/SiO_2 overcoat layer thicknesses if done with great care and read out under a

magnifying glass. For double layers on silicon substrates, the final values in terms of wt % phosphorus were about 10% lower than those obtained by the standard technique. The film thicknesses were also similarly lower (Table 2). For IC pellets, the results obtained were within ±25% of those obtained by the standard technique (Table 3).

It can be concluded that the simplified technique is adequate for some applications where lower precision (±25%) is acceptable. The time savings are considerable, and the procedure is not tedious. The

Table 2—Examples of Simplified Techniques and Repeatability of Talysurf Thickness Measurements Using PSG/SiO_2 Double Layers on Si

Sample No.	Thickness (Å)		P-Etch Time (sec)			PSG Etch Rate (Å/sec)	Composition	
	SiO_2 Top	PSG Bottom	Total	SiO_2	PSG (diff.)		wt % P	Mol % P_2O_5
A	3000	4400						
	2800	4900						
	3100	4500						
	2930 av.	4600 av.	317	183	134	34	2.3	2.3
B	3000	4800						
	2700	5200						
	2600	5000						
	2900 av.	5000 av.	328	181	147	34	2.3	2.3
C	2700	4200						
	3000	4000						
	3400	4000						
	3030 av.	4070 av.	258	190	68	60	4.1	4.2
D	3000	4000						
	2700	4000						
	2800	4000						
	2830 av.	4000 av.	254	177	77	52	3.7	3.7
E	1100	5800						
	1200	5800						
	1150 av.	5800 av.	167	72	95	61	4.2	4.3
AWF-1	2300	4600						
	2200	4900						
	2100	4700						
	2200 av.	4730 av.	165	138	27	175	7.5	8.1

thickness of the dense SiO_2 layer beneath the glass passivation overcoat is readily measurable by both techniques, but the simplified technique has an added advantage in that the thickness of the aluminum metallization can be measured from the trace across glassed interconnect lines.

The data presented in Tables 2 and 3 also demonstrate that both analytical techniques described are well suited for determining the composition and layer structure of films deposited on silicon wafer

Table 3—Comparison of Results Obtained by Standard[1] and Simplified[2] Techniques of Analysis for PSG/SiO_2 Layer Structures on Si

Sample No.	Analysis Technique	Thickness (Å)		Phosphorus in PSG (wt %)
		SiO_2 Top	PSG Bottom	
F	Standard	1900	4610	4.1
	Simplified	1600	4300	3.7
G	Standard	2185	4510	4.0
	Simplified	1800	4350	3.7
H	Standard	1900	4220	4.6
	Simplified	2000	3550	4.0

[1] Data based on curves from 7 to 8 separate pairs of measurements of etch time and residual film thickness by fringe counting.
[2] Data based on single etch time and 2 to 3 Talysurf thickness traces.

pieces. In fact, we have made extensive use of these techniques as a convenient process control test in CVD development and production work.

6. Application of the Method for Comparative Analysis of IC's

A variety of commercially available and representative IC's from several different suppliers was selected for a comparative analysis. All types were overcoat passivated with SiO_2 and/or PSG, and were plastic encapsulated. The integrity, layer structure, and composition of the overcoat layers were analyzed as described using the standard

Table 4—Comparison of Results Obtained by Standard[1] and Simplified[2] Techniques of Analysis for PSG/SiO_2 Structures on IC Chips

IC Pellet Analysis No.	Analysis Technique	Thickness (Å)		PSG Etch Rate (Å/sec)	Phosphorus in PSG (wt %)
		SiO_2 Top	PSG Bottom		
1	Standard	1425	4300	48	3.3
	Simplified	1500	3500	41	2.8
2	Standard	2660	4610	51	3.5
	Simplified	2670	4000	72	4.6
3	Standard	4750	0	16[3]	0
	Simplified	5100	0	17[3]	0
4	Standard	4180	4400	42	3.0
	Simplified	4000	4000	44	3.2

[1] Data based on curves from 8 to 17 pairs of measurements of etch time and residual film thickness by fringe counting.
[2] Data based on single etch time and 2 to 3 Talysurf thickness traces.
[3] SiO_2 etch rate.

technique. In most cases, two to six individual devices of a given passivation type were analyzed to derive the average values summarized in Table 5. The column headings of this table are defined as follows:

[1] "Passivation type" refers to a given type of passivating overcoat, regardless of type of IC. Suppliers may use several types of passivating overcoats for different IC's, or for the same IC's of different manufacturing dates. The grand average for a given supplier's product would not be meaningful because of the wide spread in the data due to the existing variations of overcoat systems. Averages were therefore taken only for groups of IC's whose passivating overcoats had closely similar characteristics.

[2] "Pinholes in overcoat" refers to those over the aluminum metallization only. They were made visible by immersing the devices in hot aluminum etch as described in Section 4.1.

[3] "Layer composition" was determined without densifying the samples.

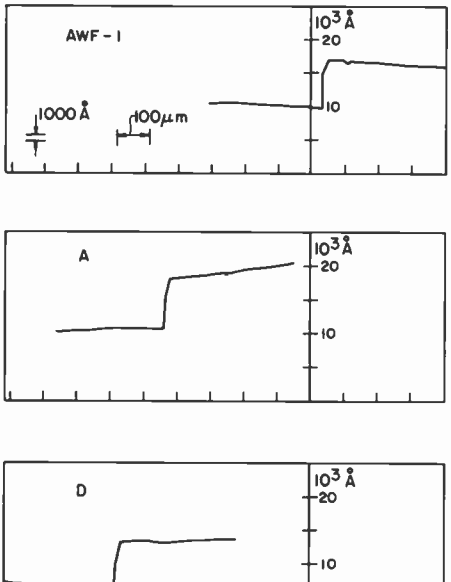


Fig. 13—Reproduction of three typical Talysurf traces from samples of step-etched PSG/SiO_2 double layers on silicon selected from Table 1. Top layer is SiO_2; bottom layer is PSG. Vertical magnification is 20,000×; horizontal magnification is 100×.

Table 5—Comparative Analysis of IC Glass Overcoats

Manufacturer Code	Passivation Type*	Pinholes in Overcoat,* # per pellet	SiO_2 Top Layer Thickness (Å)	PSG Layer Thickness (Å)	Layer Composition*	
					wt % P	mol % P_2O_5
A	A-1	0–many	7,500		0	0
				7,500**	9.7**	10.8**
B	B-1	0–4	0	7,900	7.7	8.3
B	B-2	6–many	0	7,750	4.2	4.3
B	B-3	40	≤1,000		0	0
				5,500	1.9	1.9
B	B-4	0	0	7,300	6.1	6.3
C	C-1	many	4,750	0	0	0
C	C-2	0–many	1,840		0	0
				4,385	3.3	3.4
C	C-3	2	1,280		0	0
				5,880	2.8	2.8
C	C-4	20–many	4,180		0	0
				4,400	2.9	2.9
D	D-1	0	2,000		0	0
				12,000	3.8	3.8
D	D-2	0	1,300		0	0
				4,670	4.2	4.2
			3,400†		0	0
E	E-1	15	13,000	0	0	0
E	E-2	many	7,850	0	0	0
F	F-1	18	7,340	0	0	0

* See Section 6 of text for explanation of these column headings.

** This PSG layer is underneath the aluminum metallization. The glass is in a densified state as it had been heated to fusion temperature to produce a gradually tapered slope. Etch rate analysis was based on PSG standards fused at 1000°C for 1 hour in N_2.

† Bottom layer of a tri-layer structure.

The results from this limited number of representative devices, principally manufactured in 1973, show that a wide variation of layer combinations, layer thicknesses, and PSG compositions existed, not only from one manufacturer to another, but also within the products of a given manufacturer. The same holds for the pinhole density, which ranges from zero to many per device pellet. Pinholes in the glass overcoat may have been caused by aluminum grain growth during CVD or by photolithographic contact printing.[1,3,8,18,19] No microcracks were found in any of the devices tested, probably because none of these plastic-encapsulated types had undergone high-temperature heat treatments subsequent to CVD glassing, which is usually needed only for hermetic types. It is apparent that, when the devices were fabricated, manufacturers of IC's lacked either the necessary knowledge to decide what properties of the overcoat passivation should be specified and employed, or the process control techniques for effectively monitoring the CVD processes, or both. Process design engineers have only recently begun to realize the importance of these matters in achieving a consistently high degree of product reliability. Recently reported[19] analysis results on localized structural defects in various types of glass overcoats on bipolar and CMOS devices metallized with either aluminum or gold-refractory metal tend to confirm our findings; in addition to pinholes, defects frequently encountered include cracks in the glass and improper metal line coverage.

7. Application of Method for Characterizing Other Types of Dielectric Layers

The selective etching system described so far has been designed specifically for analyzing layer composites of PSG and SiO_2. However, the applicability of the method can be extended to other dielectric layer systems, such as layers of binary CVD borosilicate glass and SiO_2, by use of suitable calibration curves.[20] It may be necessary to ascertain first the elemental composition of an unknown dielectric by a preliminary qualitative analysis, preferably by scanning Auger microprobe analysis.[6,7] For this purpose, it is usually best to select relatively large overcoated metallization areas, such as capacitors, to determine the composition of the dielectric overcoat without interference from the doped oxide sub-layers.

The method can also be useful for qualitatively characterizing layer composites consisting of single component materials, such as CVD Al_2O_3 on SiO_2 or low-temperature deposited silicon nitride on SiO_2. Two examples are presented in Fig. 14 showing etching characteristics of silicon nitride overcoat films deposited at 300°C by the re-

action of silane with ammonia or nitrogen in a rf glow discharge.[21,22] One of the graphs shows a silicon nitride film of uniform composition deposited over a dense SiO_2 layer. The other shows a silicon nitride deposit having two distinctly different etch rate components, indicating compositional differences that have implications pertaining to the deposition process.

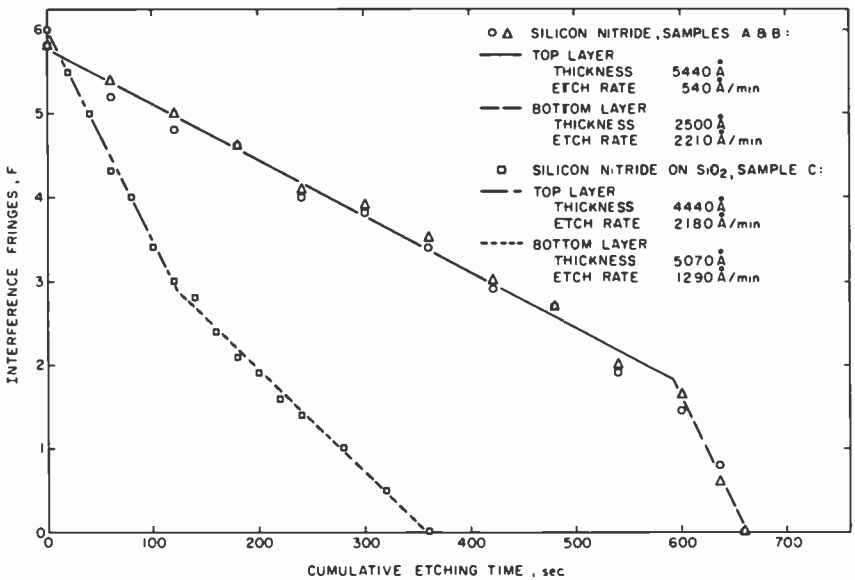


Fig. 14—Application of selective etching method using buffered HF at 25°C for characterizing plasma-deposited silicon nitride layers. The plots for two codeposited samples A and B show that the layers consist of a slow-etching and a fast-etching component, with good agreement between the two samples. Structure C consists of dense SiO_2 covered by a silicon nitride layer of different composition than in A and B.

8. Summary and Conclusions

A general method based on selective chemical etching has been devised to determine the quality of passivation overcoat layers deposited over metallized IC's. The method has been specifically optimized for quantitatively analyzing single-layer and multilayer structures of both SiO_2 and PSG on aluminum-metallized individual IC pellets, and assesses the chemical composition, the component layer structure, and the integrity of the dielectric overcoat in terms of the num-

ber of defects such as pinholes and microcracks over the aluminum metallization. The primary passivation layers underneath the metallization can be readily characterized at the same time the overcoat analysis is performed.

Two techniques for determining layer thickness and composition have been developed and applied. In the standard technique the types and thicknesses of combination layers are determined from graphical plots of differential etch rates. The phosphorus content in PSG layers is then read off a calibration curve that relates the etch rate with the % P. This technique is precise, accurate, and reliable, but somewhat time-consuming to perform.

The second technique is considerably simplified and faster in that the precision etching requires only measurement of the total etch time for the overcoat, followed by one or two contour measurements with a stylus instrument. However, the profile of the etched step must be sufficiently sharp to allow graphical resolution into the component layers, which is not always the case. This technique may be recommended for cases where lower accuracy and precision are acceptable, and for routine applications where many samples with very similar layer composites are to be examined.

The basis for determining layer structure and composition is quantitative selective etching under isothermal conditions. We have shown that isothermal etch-rate tests are simple and convenient; densifying the films before etching renders the etch rate a unique function of the composition only, since dynamic effects in the as-deposited films due to film stress and density anneal on heating. Generally applicable calibration curves have been presented relating etch rates of as-deposited and of densified CVD PSG and SiO_2 films with composition established by primary wet chemical analysis, and also with relative film density. Furthermore, the etch-rate results can be used to estimate the hydride gas composition that was used in the manufacture of the device. The techniques described are therefore well suitable for determining the composition and layer structure of films deposited on silicon control chips for monitoring the CVD processes as well as for IC pellet analysis.

Procedural details have been provided to enable other workers to apply the method in the laboratory. Recommendations on pellet decapsulation have also been presented, since very little published information is available on this essential prerequisite for analysis.

The method has been successfully applied to the analysis of commercial IC's from various manufacturers, including complex structures consisting of several component layers. The results of this survey have been tabulated and discussed, demonstrating that a wide

variety of layer combinations, thicknesses, and PSG compositions have been employed, often with poor process control.

Application of the method of selective etching can be extended to the characterization of other types of dielectric layer structures. Examples have been presented for layers consisting of silicon nitride deposited at low temperature by plasma reactions.

Acknowledgments

I wish to thank Robert D. Vibronek and C. Edwin Tracy for their technical assistance in this project, John Sabo and Bernard L. Goydish for wet chemical analysis, and George R. Auth for the Talysurf measurements. I am indebted also to Herbert Foxman for his expert advice on decapsulation procedures and for providing the photograph of a decapsulated device, and to George L. Schnable and Norman Goldsmith for critically reviewing the manuscript.

Appendix 1—Decapsulation Techniques

a. Using a drill press, cut a hole in the top center of the plastic package just deep enough to reach or cut the bond wires. Alternatively, use a small electric rotary hand grinder to produce the opening by hand. The diameter of the hole should extend across the lengthwise center third of the package. Rinse with acetone and air-dry.

b. Dissolve the epoxy–novolac (or phenolic) based encapsulant by immersing the package on a tungsten wire in white fuming nitric acid (90%) at a temperature in the range of 50° to 90°C just long enough to expose the IC pellet. Immersion time for epoxies at 90°C is typically 25 to 50 seconds; much longer periods may be required for phenolics, depending on composition. During this entire operation strict safety precautions must be observed (goggles, rubber gloves, exhaust hood). Remove the sample and rinse with a jet of acetone. Rinse with water and then soak it for at least one minute in fresh acetone. Blow dry with clean, compressed air and inspect under the microscope. If necessary, repeat the acid treatment until the chip surface is fully exposed.

c. Junction coatings consisting of anhydride-cured epoxy resins are frequently used to protect the chip before plastic encapsulation. These are resistant to nitric acid. If present, dissolve them by immersing the oven-dried sample on a tungsten wire in concentrated (97%) sulfuric acid heated to 150°C under a stream of dry nitrogen (to exclude water vapor) until the device pellet is completely freed of

organic materials; this may require extraction periods totaling typically 7 to 15 minutes. Again, strict safety precautions as noted above must be observed. After 6 to 7 minutes of extraction, rinse the sample with a jet of acetone, soak it for at least one minute in fresh acetone, blow dry and inspect. Continue the acid treatment if necessary.

d. Remove encapsulants based on silicone resins by immersing the sample in 1,1,3,3-tetramethyl-guanidine at 85° ± 10°C in a covered beaker. Check every 30 minutes until the encapsulant is removed. Then rinse in running water and dry in acetone.

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Contact Resistance of Metal–Silicon Systems at Microwave Frequencies

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Abstract—Contact resistance of silicon to various metal systems was studied in actual device configurations in the frequency range of 500–2000 MHz. The experiments were made by using standard microwave Q measurement techniques of p^+nn^+ and p^+pn^+ multi-layer, all-epitaxially-grown, silicon diodes under high-field reverse-bias conditions. Experimental results obtained with Au-Cr-Si, Au-Ti-Si, and Au-Cr-Pd_2Si-Si systems are presented and discussed in terms of the device performances of diodes utilizing these metal contact systems.

1. Introduction

Electrical properties of semiconductor devices are often strongly affected by the metallic contacts placed next to the semiconductor layers. Thus, it has become increasingly important to construct ohmic, very-low-resistance contacts to silicon and to measure the contact resistance involved accurately. Voluminous work has been published dealing with the theory and measurement of the dc characteristics of the metal–semiconductor junction.[1–7] Comparatively little work, however, has been addressed to the fabrication and characterization of ohmic low-resistance contacts of silicon microwave devices.

Eng[8] has considered the various approaches for measuring the series resistance of the varactor diode at microwave frequencies. He concluded that the resonant-cavity method of evaluation of Q may be

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the best because of the ease of accomplishing the measurement and the accuracy and reproducibility of the results. His results indicated that the equivalent series resistance was essentially independent of frequency above 500 MHz.[8,9] Inal and Toker[10] in a later paper further showed that the varactor-diode resistance is frequency independent from 300 MHz on up. In a recent publication, Ohtomo[11] reported that the series resistance of silicon Impatt diodes was not frequency dependent in the 8–12 GHz region.

Three silicon microwave devices, p-i-n, varactor, and Impatt diodes, rely critically on the metal–semiconductor contact technology. The ultimate performance of all three types of diodes is limited by the metal–silicon contact resistance involved, even though for Impatt diodes an optimum impurity profile must be provided to insure the proper operation. This paper presents the results of contact resistance measurement on metal–silicon systems of actual devices under normal operating conditions using the resonant-cavity method. The measurement frequencies were in the UHF and L-band regions. All three types of above-mentioned diodes were evaluated; and the contact resistances measured were correlated with the performances of the respective devices.

The metal–silicon systems studied include gold-chromium-silicon gold-titanium-silicon, gold-palladium-chromium-silicon, and gold-chromium–palladium silicide-silicon. These systems were chosen because they are the most commonly used and potentially useful systems for fabrication of silicon microwave devices.

2. Experimental Method

All the diodes measured were fabricated from epitaxially grown multilayer n^+pp^+ or n^+np^+ structures on a (100) oriented n^+ silicon substrate by silane pyrolysis in hydrogen. Diborane (B_2H_6), arsine (AsH_3), and phosphine (PH_3) were used to achieve the desired impurity concentration in the various epitaxial layers of the silicon structure. The basic processing steps for fabrication of the various Impatt, varactor, and p-i-n diodes are the same as those described in an earlier paper.[12]

The metallization of silicon layers is described here in some detail in order to precisely state the conditions under which the metal–silicon contact is formed. The silicon surface to be metallized is first cleaned in hot sulphuric-acid–hydrogen-peroxide–water mixture followed by a distilled water rinse, hydrofluoric-acid–water dip, and distilled water rinse. The silicon wafer is then spun dry and placed immediately into the vacuum chamber. All metal layers except palladi-

um silicide were vacuum deposited at 150°C and at a pressure less than 2×10^{-6} Torr. In the case of palladium silicide, palladium is first vacuum deposited onto silicon at 250°C and then annealed at the same temperature for a period longer than that required to convert to palladium silicide, in accordance with Bower et al.[13]

The test diodes were mounted individually using soft solder in a high-quality metal ceramic package. Six 25-μm diameter gold bond wires were used to connect the top metal contact to the lip of the package. The number of bond leads used, therefore, exceeds that required for making an accurate measurement.[14] The experiment was carried out in a resonant cavity at frequencies of from 700 to 1700 MHz using standard microwave Q-measurement techniques[15,16] under reverse-bias conditions. The Q value of the packaged diode is calculated using the Q value of the empty rf coaxial cavity at the

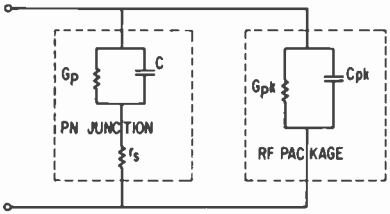

Fig. 1—Equivalent circuit of packaged p^+n or n^+p junction.

same frequency as the reference. The equivalent circuit of a packaged p^+n or n^+p junction is shown in Fig. 1. The relationship between the measured Q_d of the diode and the diode series resistance r_s is:

$$Q_d = \frac{\omega\{C + C_{pk}[(1 + r_s G_p)^2 + \omega^2 C^2 r_s^2]\}}{G_p(1 + r_s G_p) + \omega^2 C^2 r_s + G_{pk}[(1 + r_s G_p)^2 + \omega^2 C^2 r_s^2]} \quad [1]$$

where C is the depletion capacitance, C_{pk} is the package capacitance ($G_{pk} \leq 10^{-10}$ mho is the package shunt conductance), $G_p \leq 10^{-10}$ mho is the shunt conductance of the p-n junction, and ω is the radian frequency at which the Q measurement was made over the range 700–1700 MHz. Since r_s is less than 1 ohm, $r_s G_p \ll 1$, $\omega^2 C^2 r_s^2 \ll 1$, and $\omega^2 C^2 r_s^2 \gg G_p$ or G_{pk}, Eq. [1] can be reduced to:

$$Q_d = \frac{(1 + C_{pk})/C}{\omega C r_s}. \quad [2]$$

The Q factor for these low-leakage diodes in the microwave range is governed only by the depletion capacitance and the series resistance. The series resistance r_s is therefore:

$$r_s = \frac{(1 + C_{pk})/C}{\omega C Q_d}. \qquad [3]$$

The series resistance of the diode evaluated from the Q factor measured at a reverse bias voltage higher than or equal to that required to completely deplete the active layer represents the practically achievable contact resistance r_{sc} of the metal–semiconductor system. The correction due to the series resistance of the p^+ and n^+ layers is usually quite small. Using the value of contact resistance r_{sc} thus calculated, the average specific contact resistance $\bar{\rho}_s$ can be determined by:

$$\bar{\rho}_s = r_{sc} \frac{A}{2} \qquad [4]$$

where A is the cross-sectional area of the diode.

The average specific contact resistance $\bar{\rho}_s$ is used as the merit indicator for comparing various metal–silicon systems. It is related to the specific contact resistances of the metal to the n^+ and p^+ silicon layers as follows:

$$\bar{\rho}_s = \frac{\rho_{sn^+} + \rho_{sp^+}}{2} \qquad [5]$$

where ρ_{sn^+} = specific contact resistance of metal to n^+ silicon layer
ρ_{sp^+} = specific contact resistance of metal to p^+ silicon layer

3. Experimental Results

The measured average specific contact resistance $\bar{\rho}_s$ of gold-chromium-silicon, gold-titanium-silicon and gold-chromium-palladium silicide-silicon systems are given in Table 1. Dopants of the n^+ and p^+ layers as well as the larger resistivities are specified.

The dependence of contact resistance r_{sc} on cross-sectional area A of a gold-chromium-silicon system is shown in Fig. 2. The p^+ layer is boron doped and has a resistivity of 0.001 ohm-cm; the n^+ layer is arsenic doped and has a resistivity of 0.003 ohm-cm. A scale of diameter in mils corresponding to the various values of area A is also provided for the rapid estimation of contact resistance involved for any given-size diode. The effect of the thickness of the metal layer in direct contact to silicon on the contact resistance for the gold-titanium-silicon system is presented in Table 2.

The variation of specific contact resistance with the resistivity and dopants of the n^+ layer, together with the device performance as an Impatt oscillator[12] using the gold-chromium-silicon system, is given in Table 3. Table 4 compares the measured specific contact resistance

Table 1—Specific Contact Resistance of Metal–Silicon Systems

Metal–Silicon System	p^+ Layer Dopant Resistivity, ohm-cm	n^+ Layer Dopant Resistivity, ohm-cm	Average Specific Contact Resistance, $\bar{\rho}_s$, ohm-cm^2
Au-Cr-Si	Boron 0.001	Arsenic 0.003	12×10^{-6}
Au-Ti-Si	Boron 0.001	Arsenic 0.003	37×10^{-6}
Au-Cr-Si	Boron 0.001	Phosphorus + Arsenic 0.0015	7×10^{-6}
Au-Cr-Pd_2Si-Si	Boron 0.001	Phosphorus + Arsenic 0.0015	8×10^{-6}

Table 2—Dependence of Specific Contact Resistance on Thickness of Titanium Layer for Gold-Titanium-Silicon System

Thickness of Titanium Layer, Å	p^+ Layer Dopant Resistivity, ohm-cm	n^+ Layer Dopant Resistivity, ohm-cm	Average Specific Contact Resistance, $\bar{\rho}_s$, ohm-cm^2
20	Boron 0.001	Arsenic 0.003	36×10^{-6}
100	Boron 0.001	Arsenic 0.003	38×10^{-6}

Table 3—Dependence of Specific Contact Resistance on Resistivity and Dopants of n^+ Layer and Resulting Device Performance for Gold-Chromium-Silicon System

p^+ Layer Dopant Resistivity, ohm-cm	n^+ Layer Dopant Resistivity, ohm-cm	Average Specific Contact Resistance, $\bar{\rho}_s$, ohm-cm^2	Device Performance as an IMPATT Oscillator[12]		
			Max. Eff. η, %	CW Output Power, mW	Freq. GHz
Boron 0.001	Arsenic 0.003	12×10^{-6}	9.2	555	29.6
Boron 0.001	Phosphorus 0.0015	4×10^{-6}	10.9	460	35.3
Boron 0.001	Phosphorus + Arsenic 0.0015	7×10^{-6}	9.7	565	32.5

Table 4—Specific Contact Resistance and Device Performance as Related to Conditions of Vacuum Deposition of Metals for the Gold-Palladium-Chromium-Silicon System

Background Pressure During Vacuum Deposition of Metal Layers onto Silicon	p^+ Layer Dopant Resistivity, ohm-cm	n^+ Layer Dopant Resistivity, ohm-cm	Average Specific Contact Resistance, $\bar{\rho}_s$, ohm-cm^2	Device Performance as Impatt Oscillator		
				Max. Eff., η, %	CW Output Power, mW	Freq. GHz
10^{-6}	Boron 0.001	Arsenic 0.003	7×10^{-6}	8.7	500	22.05
10^{-5}	Boron 0.001	Arsenic 0.003	42×10^{-6}	4.7	240	19.23

with the device performance as an Impatt oscillator observed under two different conditions of vacuum deposition of the metals for the gold-palladium-chromium-silicon system.

The specific contact resistance and device performance of a number of the regular p^+nn^+ varactor diodes and the back-to-back $p^+nn^+p^+$ varactor diode is given in Table 5. The effective contact resistance r_{sc} of the $p^+nn^+p^+$ diode referred to in Table 5 includes the resistance of the p^+, n^+, p^+ layers plus the extra series resistance of the p^+n^+ junction.

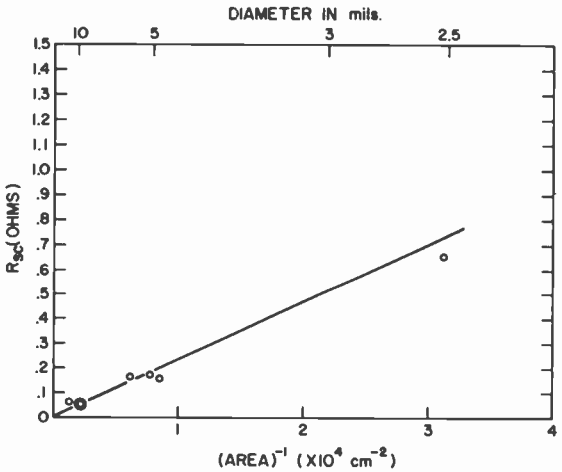

Fig. 2—Dependence of contact resistance on cross-sectional area of a gold-chromium-silicon system.

4. Discussion

All our series resistance measurements were made in the frequency range of 700 to 1700 MHz and they have been considered to be frequency independent in computing the value of specific contact resistance listed in Table 1. This was justified by the earlier work of Eng,[8,9] Inal and Toker,[10] and Ohtomo,[11] together with the observation that identical results of series resistance of p-i-n diodes were obtained at 600 and 1000 MHz under heavily forward biased conditions. The experimentally determined average specific contact resistance for gold-chromium-silicon and gold-chromium-palladium-silicide-silicon systems (Table 1) is within the realm of the expected value calculated from theory for the dc case by Chang, Fang, and Sze[3] using a

Table 5—Specific Contact Resistance and Device Performance of Silicon Varactor Diodes

Varactor Structure	Metal-Silicon System	p^+ Layer Dopant Resistivity, ohm-cm	n^+ Layer Dopant Resistivity, ohm-cm	Average Specific Contact Resistance, $\bar{\rho}_s$, ohm-cm^2	Device Performance as Varactor		
					$Q_{low\ bias}$	$Q_{high\ bias}$	$\frac{C_{low\ bias}*}{C_{high\ bias}}$ Capacitance Ratio
p^+nn^+	Au-Ti-Si	Boron 0.001	Arsenic 0.003	33×10^{-6}	60 at 3 Volts 332 MHz	476 at 35 Volts 890 MHz	5.0
p^+nn^+	Au-Cr-Si	Boron 0.001	Arsenic 0.003	12×10^{-6}	108 at 3 Volts 323 MHz	1453 at 35 Volts 858 MHz	5.2
p^+nn^+	Au-Cr-Si	Boron 0.001	Arsenic 0.003	12×10^{-6}	200 at 0.6 Volt 349 MHz	1260 at 35 Volts 791 MHz	4.5
$p^+nn^+p^+$	Au-Cr-Si	Boron 0.001	Arsenic 0.003	27×10^{-6}†	130 at 0.5 Volt 412 MHz	640 at 35 Volts 793 MHz	4.3

*Package capacitance of 0.23 pF included.
†Effective average contact resistance including the contribution of the resistance p^+,n^+,p^+ layers as well as the p^+n^+ junction.

barrier height of 0.68 eV for Cr-n-Si[17] and 0.745 eV for Pd_2Si-n-Si.[18] In addition, the average specific contact resistance $\bar{\rho}_s$ for gold-chromium-silicon agrees very well with our own dc measurement on bulk silicon wafers, i.e., ρ_{sp^+} of 9×10^{-6} ohm-cm^2 for a p^+ wafer of 0.001 ohm-cm resistivity and ρ_{sn^+} of 22×10^{-6} for an n^+ wafer of 0.008 ohm-cm resistivity. The value reported here is consistent with the dc specific contact resistance obtained earlier by Hooper, Cunningham, and Harper[5] on Cr-Si. The average specific contact resistance for the Au-Cr-Pd_2Si-Si system listed in Table 1 falls in between the values of dc contact resistance measured for the Pd_2Si-Si contacts by Kircher[18] and by Buckley and Moss.[19] Furthermore, all of the resistance values are within the same order of magnitude.

The average specific contact resistance measured for the gold-titanium-silicon system is much higher than the dc measurement on bulk silicon wafers. A specific contact resistance ρ_{sp^+} of 6×10^{-6} ohm-cm^2 was measured on a 0.001 ohm-cm p^+ wafer, and ρ_{sn^+} of 14×10^{-6} ohm-cm^2 on a 0.008 ohm-cm n^+ silicon wafer in the dc case. In contrast to the Au–Cr–Si case, a factor of 4 deterioration was observed for the microwave contact resistance of a real diode to that of the dc contact resistance between titanium and a bulk silicon wafer. The mechanism for this large deterioration in contact resistance is firmly believed to be a chemical attack on titanium during the silicon-diode definition step of our processing procedure. Hydrofluoric-acid–nitric-acid in the proportion of 3 to 97 was used to define the silicon diode, and titanium is known[20] to dissolve in HF and hot HNO_3. This serves to illustrate the importance of device processing in affecting the performance of the finished diode. In this particular case, even though the measured dc contact resistance of Au-Ti-Si is less than that of Au-Cr-Si, the contact resistance observed in actual microwave devices is lower for the latter.

The contact resistance r_{sc} for Au-Cr-Si is shown to depend linearly on the reciprocal of area over the whole range of diode diameters of practical interest (see Fig. 2). The various values of r_{sc} used in the plot for Fig. 2 are measured throughout the frequency range of 790 MHz to 1500 MHz, and no corrections with respect to frequency are made. The reasonable linear relationship between r_{sc} and A^{-1} together with the good agreement between the dc and microwave measured values of specific contact resistance further substantiates the validity of the contention that the series resistance is frequency independent.

Thickness of the contact metal layer in the case of an Au-Ti-Si system does not affect the measured contact resistance, which indicates that the contact resistance is indeed dominated by the Ti-Si contact, as would be expected. The specific contact resistance should be high-

ly dependent on the resistivity of the silicon, regardless of the particular metal contact, in accordance with both the theoretical treatments[3,4,6] and the experiment findings.[5,21,22] Such a dependence was observed and tabulated in Table 3. The ratio of the average specific contact resistances between an Au-Cr-Si system containing an arsenic doped (0.003 ohm-cm) n^+ layer and one containing an arsenic-plus-phosphorus-doped (0.0015 ohm-cm) n^+ layer is about the same as the ratio of the resistivities of the two n^+ layers. This is in excellent agreement with the conclusions made by Hoare[22] that the contact resistance has been shown to be closely proportional to the bulk resistivity of the silicon. Nevertheless, the considerable lower value of average specific contact resistance for the case containing the phosphorus-doped n^+ layer (at a resistivity of 0.0015 ohm-cm) than for the case containing the phosphorus-plus-arsenic-doped n^+ layer with the same resistivity points to the preeminence of the various molecular interactions involved at the actual metal–silicon junction.

The performance of Impatt oscillators, as shown clearly in Table 3, corresponds reasonably well with the measured contact resistance. Both the device performance and the measured average specific contact resistance compare favorably with the S3019 Si Impatt's measured by Ohtomo.[11] He reported an efficiency of 5.8% and a series resistance at breakdown of 0.67 ohm (corresponding to $\bar{\rho}_s$ of 67×10^{-6} ohm-cm^2) for one diode and an efficiency of 6.3% and a series resistance at breakdown of 0.53 ohm (corresponding to $\bar{\rho}_s$ of 63×10^{-6} ohm-cm^2) for another diode. Furthermore, the device performance and the contact resistance of two batches of diodes fabricated under conditions of precisely controlled and nominally controlled vacuum deposition of metals are compared in Table 4. The importance of metal–silicon contacts in influencing the performance of Impatt oscillators cannot be over-emphasized.

The performance of a varactor is characterized by, among other things, the Q factor, the usable capacitance tuning ratio, and the maximum rf signal-handling capability in terms of peak-to-peak voltage swing. Table 5 lists the first two factors of the device performance as related to the measured contact resistance for two different varactor structures, the normal p^+nn^+ type and the back-to-back $p^+nn^+p^+$ type. The normal p^+nn^+ type diodes all have an rf signal-handling capacity of approximately 2 volts (peak-to-peak voltage swing), whereas the $p^+nn^+p^+$ type diode has a capacity of approximately 5 volts. The particular $p^+nn^+p^+$ diode has 2.5-volt and 42-volt breakdown back-to-back junctions. The $p^+nn^+p^+$ type varactor diode has a much improved rf signal handling capability at the expense of a moderate lowering of the Q factor. It appears that, in this particular case,

the forward-biased extra p^+n^+ junction has a series resistance almost identical to that of a metal-silicon junction.

The merit of a p-i-n diode is almost exclusively expressed in terms of series resistance at a specific current level. The contact resistance, which is independent of current density[7] and ever present, thus constitutes the most important figure of merit for the finished p-i-n diode. In addition, parameters such as insertion loss, isolation, and power dissipation of a circuit containing p-i-n diodes depend greatly on the diode's resistance.[23]

Acknowledgment

The authors are grateful to G. W. Looney, H. L. Davis, A. F. Young, R. Chamberlain, and O. Gervasoni for their excellent technical assistance.

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Noise Performance Factors in Television Tuners

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Abstract—The optimization of television tuner noise figure requires a simple means of recognizing the effect of component parameters on noise performance. Graphs are presented that quickly and precisely show the influence of amplifier gain and noise figure, image rejection, filter element Q's, and mixer noise figure on the overall noise performance of the television tuner.

Introduction

Optimization of a system noise figure requires a simple means of recognizing the effect of component parameters on noise performance. The basic television tuner consists of a preselector, rf amplifier, post selector, and mixer as shown in Fig. 1. The noise figure and gain associated with the amplifier and mixer, along with the filter resonator Q, which determines the insertion loss and image rejection of the filter, are the most significant parameters in analyzing noise performance. Another element, the one which is in practice the limiting factor in noise performance of tuners today, is cost. A knowledge of the influence of the system parameters on noise performance, and the cost of an improvement in them, allows a logical decision to be made on the cost effectiveness and performance trade-offs for a particular tuner system. The graphs described in this paper greatly aid in the rapid evaluation of the effect of the various parameters on tuner performance.

Pre- and Post-Selector Filters

The filters, which provide selectivity and image rejection for the television receiver, usually consist of a single section preceding the rf amplifier and a double-section post selector. The combined response must provide the required image rejection and the smallest possible insertion loss. A narrow bandpass filter design, which assumes the fil-

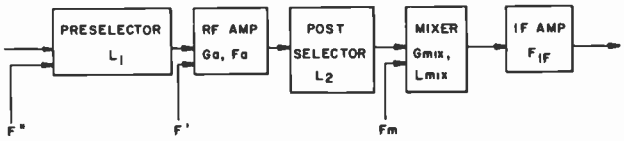

Fig. 1—Tuner system.

ter elements to be lossless, will result in an n section filter that has an attenuation, L_s, at the image frequency of

$$L_s = n \text{ (image rejection for single-pole filter) dB} \qquad [1]$$

and an insertion loss, L_0, of

$$L_0 = 0 \text{ dB}. \qquad [2]$$

When dissipative losses in the filter elements are taken into account, however, not only will the filter have insertion loss but the image injection will no longer be additive as it is in the lossless case. Cohen[1], has studied the general case of multiple resonator filters, including dissipation loss in the filter elements, and has found that an equal-element filter prototype will provide almost minimum insertion loss for a specified high attenuation at some nearby frequency. Under these conditions the relationship between the insertion loss and the loss, L_s', at the image frequency is found to be

$$L_0 = \frac{4.343n \text{ antilog } \dfrac{L_s' + 6.02}{20n}}{\omega_s Q_0} \text{ dB} \qquad [3]$$

where ω_s is the fractional image bandwidth, $(\omega_{i2} - \omega_{i1})/\omega_0$, and Q_0 is the unloaded Q of each filter section. Since the image rejection is defined as the attenuation at the image frequency with respect to the filter response at mid-band, the image rejection, L_s, in the loss element case becomes

$$L_s = L_s' - L_0 \text{ dB} \qquad [4]$$

It is important to note that Eq. [3] has a minimum value of L_0 that is a function of the number of filter sections for fixed values of L_s', ω_s, and Q_0, i.e., the insertion loss will not be the minimum value if n is too small or too large.

This relationship between the insertion loss and image rejection is brought about by the loss in the circuit elements, which is represented by the unloaded Q of the resonators. Since the Q is the basis of the discussion, it should be carefully considered. The unloaded Q of each filter section is the combined unloaded Q of the capacitance and inductance associated with the section:

$$\frac{1}{Q_0} = \frac{1}{Q_{0c}} + \frac{1}{Q_{0L}} \qquad [5]$$

where Q_{0c} is the unloaded capacitive Q and Q_{0L} is the unloaded inductive Q.

When the capacitor and inductor are lumped elements the unloaded Q values are simply defined. However, if the capacitive element is a varactor, the unloaded Q must be measured at the proper bias conditions, and the Q of the blocking capacitor, if any, must be taken into account.

$$Q_{0c} = \frac{X_B + X_V}{\dfrac{X_B}{Q_B} + \dfrac{X_V}{Q_V}} \qquad [6]$$

where X_B and X_V indicate the reactances of the blocking capacitor and varactor, respectively.

When transmission line resonators are used, the element Q's are not as simply defined.[2] The Q of any element or resonator is the ratio of the energy stored to the power dissipated in it. When lumped elements are used, the electric field is localized in the capacitive components and the magnetic field is localized in the inductive components. A transmission line, being distributed in nature, contains both electric and magnetic fields. In the commonly used configuration shown in Fig. 2, a transmission line, shorted at one end, is resonated with a lumped element capacitor or varactor. At resonance, only a portion of the maximum electric energy is stored in the capacitor. This effect must be taken into account when considering the effective capacitive Q.

The total power dissipated in the resonator is the sum of the powers dissipated in the transmission line and in the capacitor

$$P_0 = P_{0L} + P_{0c}. \qquad [7]$$

The stored energy, U, is related to the Q and the dissipated power by

$$Q_{0c} = \frac{\omega U_{0c}}{P_{0c}}$$

$$Q_{0L} = \frac{\omega U_{0L}}{P_{0L}} \qquad [8]$$

$$Q_0 = \frac{\omega U_0}{P_0}$$

Substituting these values into the equation for dissipated power gives

$$\frac{U_0}{Q_0} = \frac{U_{0L}}{Q_{0L}} + \frac{U_{0c}}{Q_{0c}}. \qquad [9]$$

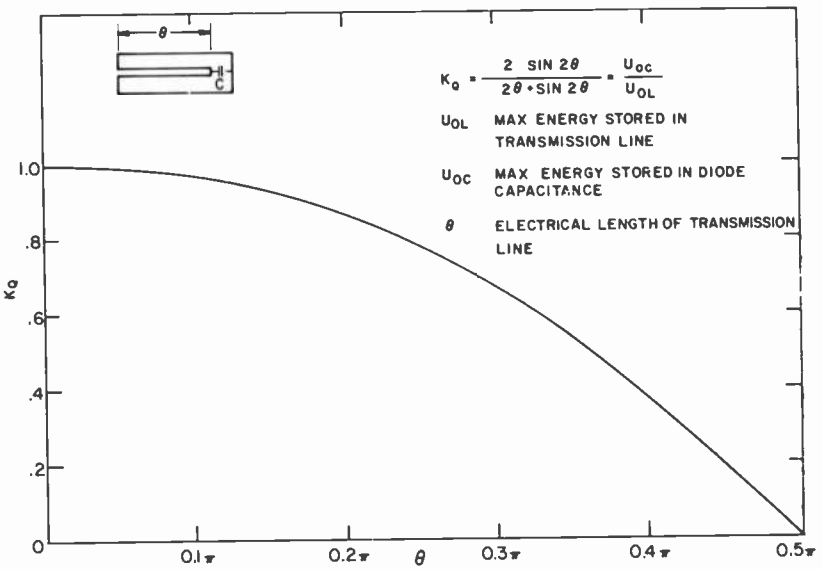

Fig. 2—Stored energy correction factor.

At resonance there exists a continuous interchange of energy between the magnetic and electric fields. At any instant of time the total energy stored in the system is equal to the maximum energy stored in the magnetic field. This occurs when the current is a maximum. Therefore

$$U_0 = U_{0L}|_{max\,I} \qquad [10]$$

and

$$\frac{1}{Q_0} = \frac{1}{Q_{0L}} + \frac{1}{Q_{0c}/K_Q} \qquad [11]$$

where

$$K_Q = \frac{U_{0c}}{U_{0L}|_{max\,I}} \qquad [12]$$

It should be noted that in the case of a lumped-element resonant system, the maximum energy stored in the magnetic field of the inductor is equal to the maximum energy stored in the electric field of the capacitor. Therefore

$$U_0 = U_{0L}|_{max\,I} = U_{0c}|_{max\,V} \qquad [13]$$

and

$$\frac{1}{Q_0} = \frac{1}{Q_{0L}} + \frac{1}{Q_{0c}} \qquad [14]$$

Comparing the Q equations for the transmission line and lumped element cases, shows that the effective capacitive Q for the transmission line resonator becomes

$$Q_{0c} = \frac{Q_{0c}}{K_Q} \qquad [15]$$

The value of K_Q can be found by calculating the energy stored in the transmission line and the capacitor for maximum current conditions.

$$U_0 = \frac{1}{2} L_L \int_0^{x_1} I(x)dx$$

$$U_c = \frac{1}{2} C[V(x_1)]^2 \qquad [16]$$

where

$I(x) = I \cos \beta x$
$V(x) = j\, IZ_0 \cos \beta x$
$Z(x) = j\, Z_{0'} \tan \beta x$
L_L = inductance per unit length
C = capacitance

The resulting value for K_Q is

$$K_Q = \frac{U_{0c}}{U_{0LImax}} = \frac{2 \sin 2\theta}{2\theta + \sin 2\theta}$$

where θ is the electrical length of the transmission line. Fig. 2 shows the relationship between the correction factor, K_Q, and the electrical length of the transmission line.[2]

The relationship between the Q values and filter performance is interpreted graphically in Fig. 3. The center of the graph consists of a plot of total loss at the image frequency as a function of a parameter

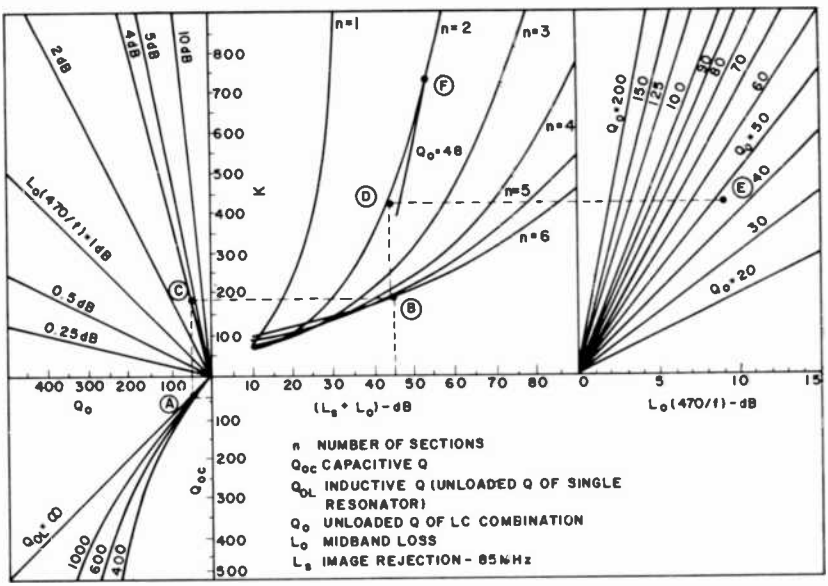

Fig. 3—*n*-section television tuner filter.

K for up to six filter sections, where K is defined as:

$$K = Q_0 L_0 \left(\frac{470}{f}\right) \qquad [18]$$

To the left is a plot of K as a function of Q_0 with $L_0(470/f)$ as a parameter. This permits the direct resolution of K into insertion loss and unloaded circuit Q. To the right, K is plotted as a function of $L_0(470/f)$ with Q_0 as the parameter.

The graphs were produced for a television channel center at 470 MHz and an image frequency 85 MHz above 470 Mhz. For the same image bandwidth centered at any other frequency, simply multiply the value of $L_0(470/f)$ by the new frequency normalized to 470 MHz i.e., f(MHz)/470. To change the image bandwidth multiply the value of $L_0(470/f)$ by $85/|f_i - f|$. In general for any half image bandwidth, $f_i - f$, and any center frequency f,

$$L_0' = L_0 \left(\frac{470}{f}\right)\left(\frac{f}{470}\right)\left(\frac{85}{|f_i - f|}\right) \text{ dB} \qquad [19]$$

where all frequencies are in MHz.

The lower left-hand plot converts the capacitive and reactive unloaded Q's to total circuit unloaded Q, i.e., Q_0.

A significant fact which is seen by inspection of the center plot is that, for a given unloaded Q, there is an optimum number of filter sections that will yield best image-rejection and insertion-loss performance. For example, if the total loss at the image frequency is 10 dB, a filter consisting of only two sections will have an insertion loss of 0.6 dB while a six-section filter will have an insertion loss of 1 dB. On the other hand a 30-dB total loss at the image frequency is best realized by a four-section filter. Table 1 provides a tabulation of total loss at the image frequency and the number of filter sections that will provide minimum insertion loss. The actual value of insertion loss will depend on Q_0.

Table 1—Number of Filters Providing Minimum Insertion Loss

Total Loss ($L_s + L_o$) dB	Optimum Number of Filter Sections
10 to 15	2
15 to 24	3
24 to 30	4
30 to 45	5

The use of Fig. 3 can best be seen by considering the following example. An electronic filter will use varactors having corrected unloaded Q's of 50 at 470 MHz. The Q of the transmission line section is 1000. The problem is to determine the optimum number of filter sections and the filter insertion loss for an image rejection of 40 dB. Table I indicates that the number of filter sections is five. Therefore

$$L_s = 40 \text{ dB}$$

$$\frac{Q_{0c}}{K_Q} = 50$$

$$Q_{0L} = 1000$$

$$n = 5$$

Since the insertion loss will be several dB, the starting value of $L_s + L_0$ should be chosen slightly higher than 40 dB. Let $L_s + L_0 = 45$ dB. The intersection of Q_{0c} and Q_{0L} values results in $Q_0 = 48$ at point

A. Point B gives the K value for $L_s + L_0 = 45$ and $n = 5$. The intersection of this K value and the Q_0 value occur at point C resulting in an insertion loss of 4 dB. The image rejection is therefore 41 dB. If the value of $L_s + L_0$ is reduced to 40 dB, the insertion loss remains at about 4 dB thus giving the required result. Therefore

$$n = 5$$

$$L_0 = 4 \text{ dB}$$

$$L_s = (L_s + L_0) - L_0 = 44 - 4 = 40 \text{ dB}$$

If n is now reduced to two sections the new K value is found at point D. The intersection of this K value and the $Q_0 = 48$ line occurs at Point E resulting in an insertion loss of 8.8 dB and an image rejection of only 35.2 dB.

$$n = 2$$

$$L_0 = 8.8 \text{ dB}$$

$$L_s = 44 - 8.8 = 35.2 \text{ dB}$$

To maintain the image rejection at 40 dB with a two-section filter is almost impossible, because the insertion loss increases much faster than the image rejection. For an insertion loss of 15 dB, $L_s + L_0$ is only 53 dB and increases to only 58 dB for an insertion loss of 23 dB.

$$L_0 = 8.8 \text{ dB} \qquad L_s = 44 - 8.8 = 35.2 \text{ dB}$$

$$L_0 = 15 \text{ dB} \qquad L_s = 53 - 15 = 38 \text{ dB}$$

$$L_0 = 23 \text{ dB} \qquad L_s = 58 - 23 = 35 \text{ dB}$$

The largest value of image rejection that is attainable for a given Q_0 occurs when the slope of the n parameter curves is the same as the slope of the Q_0 parameter curves when the abscissas (dB) scales are equal. Therefore the line corresponding to the value of Q_0, which has the slope

$$\frac{\Delta K}{\Delta(L_s+L_0)} = Q_0 \qquad [20]$$

can be overlayed on the center region of Fig. 3 and slid until the tangent point is found. This is done in Fig. 3 for this example and is found to be 38 dB with an insertion loss of 15 dB. It is important to remember that this maximum value of image rejection does not occur for minimum insertion loss.

Since many tuners are designed using a single-section preselector and double-section post selector, the insertion loss versus image re-

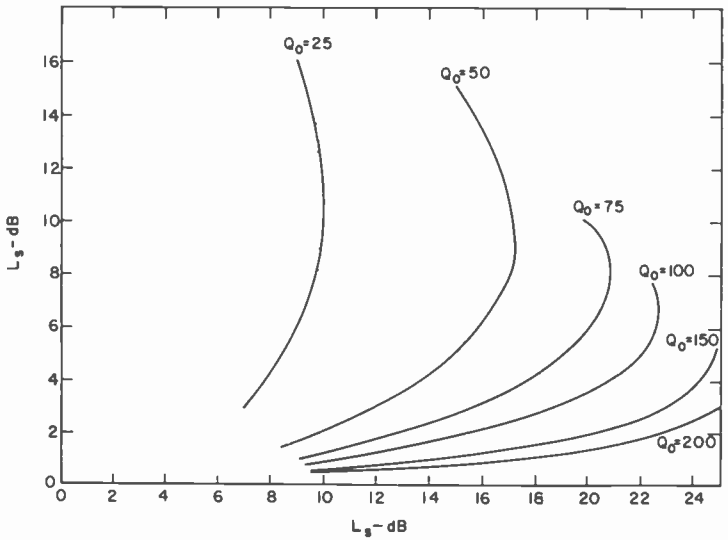

Fig. 4—Image rejection and insertion loss (one-section filter).

jection with Q_0 as a parameter is plotted in Figs. 4 and 5. Fig. 4 clearly identifies the maximum image rejection for various Q_0 values. A comparison of both plots shows that for an image rejection less than 10 dB the insertion loss for a single section is approximately the same as that for a double section. However, the image rejection for a dou-

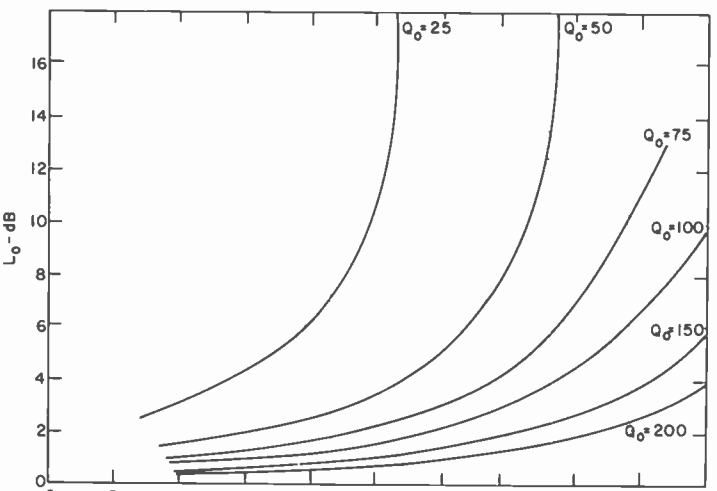

Fig. 5—Image rejection and insertion loss (two-section filter).

ble section may be increased greatly for a very small increase in total insertion loss.

Another important property of filters with dissipative losses can be seen by examining Fig. 3. A two-section filter with an insertion loss of 10 dB and $Q_0 = 50$ will have an image rejection of 36.6 dB. If the filter sections are now separated by a unity-gain amplifier, the new filter will consist of two single resonators. To maintain the same total insertion loss, let each section have 5-dB insertion loss. The image rejection per section will then be 15 dB for a total image rejection of only 30 dB compared to the original 36.6 dB. If the image rejection were held constant, then the insertion loss would have deteriorated. This is true for any number of filter sections and results because the criteria for external loading and critical internal coupling are different in the lossless and dissipative cases.

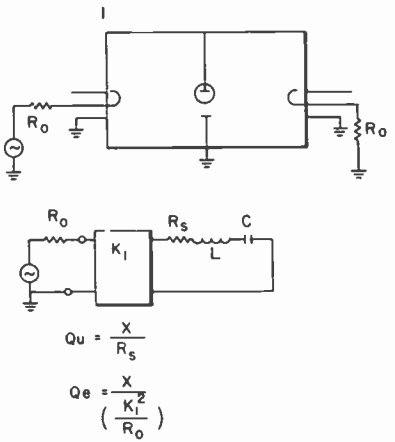

Fig. 6—Coupled cavity resonators.

To get better insight into the effect of coupling and trade off between insertion loss and image rejection, an examination of two coupled filter sections is useful. Presser originally developed a graph in the form of Fig. 3 for a symmetrical pair of cavity resonators with loop couplings.[2,3] For this case, shown in Fig. 6, the insertion loss is

$$L_0 = 20\log_{10}\left[\frac{\left(1+\frac{Q_e}{Q_0}\right)^2}{22kQ_e} + \frac{kQ_e}{2}\right] \text{dB} \qquad [20]$$

where Q_e is the external Q of each cavity and k is the coefficient of coupling between cavities. The critical coupling, k_q, between cavities is defined as

$$k_q = \frac{1}{Q_e} + \frac{1}{Q_0} \qquad [21]$$

This coupling provides minimum insertion loss for a single lumped response. Under these conditions the insertion loss becomes

$$L_0 = 20\log_{10}\left[1 + \frac{Q_e}{Q_0}\right] \text{dB} \qquad [22]$$

The image rejection for the two critically coupled cavities is

$$L_s = 10\log_{10}\left\{\left(1 + \frac{Q_e}{Q_0}\right)^2 + \left[2\frac{Q_e{}^2}{(1 + Q_e/Q_0)}\left(\frac{f_i - f}{f}\right)^2\right]^2\right\} - L_0 \text{ dB} \qquad [23]$$

Both the insertion loss and image rejection are functions of the external Q, which is a measure of the loading of each cavity, and the unloaded Q of the cavities. The value of Q_e can be changed by adjusting the external coupling loops. However, when the external coupling loops are adjusted, the internal coupling loops must also be adjusted so that critical coupling is maintained. The relationship between the coupling, insertion loss, and image rejection is now evident. The image rejection should be made as high as possible, which requires Q_e to be large compared to Q_0. To make the insertion loss low, Q_e should be small compared to Q_0. Since both these criteria are in opposition to one another, a compromise must be made.

In the case of nondissipative filter sections the cavity unloaded Q would be infinite and the insertion loss and image rejection become

$$L_0 = 20\log_{10}1 = 0 \text{ dB} \qquad [24]$$

$$L_s = 10\log_{10} 1 + 4\,Q_e\left(\frac{f_i - f}{f}\right)^4 \text{dB} \qquad [25]$$

The coefficient for critical coupling becomes

$$k_q = \frac{1}{Q_e} \qquad [26]$$

Lossless filter sections do not require a trade-off between insertion loss and image rejection because the insertion loss at a frequency f_i is a function of the external coupling only.

The requirement that these filters be tunable over an octave bandwidth resulted in a filter design that was as simple as possible, i.e., a filter that contained transfer-function poles only. However, filters that contain both poles and zeros can provide additional skirt selectivity if the zeros are placed at the image frequency. A technique that

may be used to provide an additional 6 to 10 dB of image rejection, without too much difficulty, consists of coupling the input signal to the output of the filter through an additional path.[4] The basic concept can best be seen by considering the system shown in Fig. 7. Both signals are decoupled at the input to the filter by the same amount as the image rejection of the filter. A phase shifter is added to the decoupled arm and is adjusted so that the signal appearing at port B of the adder is 180 degrees out of phase with the signal at port A. The

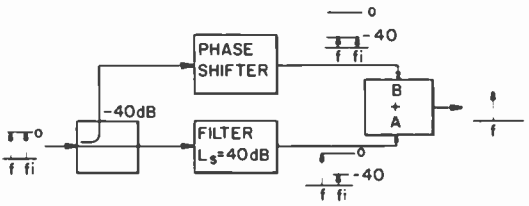

Fig. 7—Cancellation of image signal.

output of the adder consists of the vector addition of the image signal along with the vector addition of the desired signal. At the desired frequency the addition consists of adding two signals whose magnitudes are different by approximately 40 dB. The resultant is therefore the desired signal as it appeared at port A. The signal at the image frequency will be completely cancelled at the output if the phase and amplitude are adjusted correctly.

This concept, as applied to a resonant cavity or coupled transformer type structure, consists of coupling some of the input signal by means of the output coupling loop and adjusting this loop for the proper phase and amplitude relationship.

System Noise Figure

The minimum system noise figure is the noise figure of the rf amplifier. The ultimate goal is to reduce this to its lowest practical value. Optimization of the rest of the system consists of adjusting the amplifier gain, post-selector insertion loss and mixer noise figure so that the system noise figure approaches the rf amplifier noise figure.

The generalized tuner is shown in Fig. 1 along with the significant noise-figure parameters. The system noise figure, F', is given by

$$F' = L_1 \left[F_A + \frac{L_2 \left(F_{mix} + \frac{F_{IF} - 1}{G_{mix}} \right)^{-1}}{G_A} \right] \qquad [27]$$

where L_1 = preselector insertion loss, L_2 = post-selector insertion loss, G_A = rf amplifier gain, G_{mix} = mixer conversion gain, F_A = rf amplifier noise figure, F_{mix} = mixer noise figure, and F_{IF} = i-f amplifier noise figure, all expressed as ratios.

Fig. 8 can be used to quickly determine the effect of rf amplifier gain and noise figure, filter insertion loss, and mixer noise figure without having to recalculate Eq. [27] for every change. The product of system noise figure and amplifier gain expressed in dB is plotted as

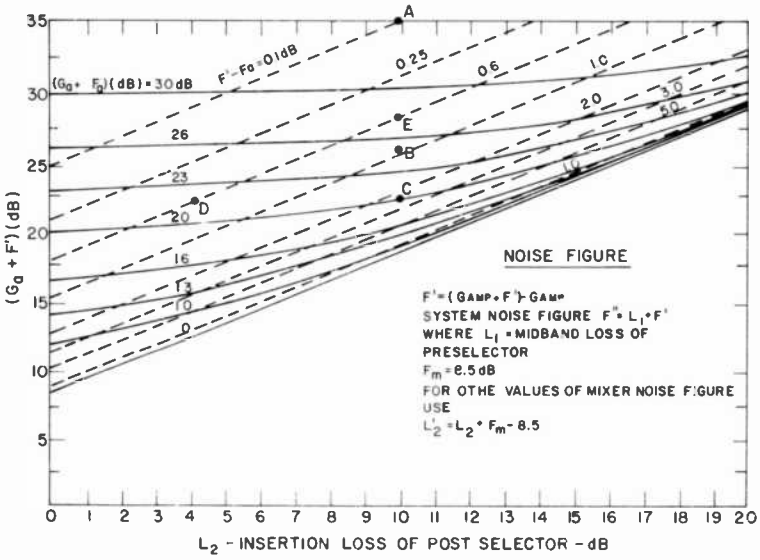

Fig. 8—System noise figure.

a function of post-selector insertion loss with the product of amplifier noise figure and gain as a parameter. The noise figure at the input to the mixer was assumed to be 8.5 dB which is a typical value in the UHF band. Since the post-selector insertion loss is directly added to this noise-figure value, any other noise figure at the input of the mixer may be accommodated by simply adjusting the value of L_2.

$$L_2' = L_2 + F_m - 8.5 \text{ dB} \qquad [28]$$

where F_m is the noise figure at the input to the mixer (dB).

The difference between the system noise figure and the amplifier noise figure, $F' - F_A$, is also used as a parameter on the same set of axis. This set of parameters is useful in determining the amplifier gain required to overcome the effect of filter insertion loss. For exam-

ple, $F' - F_A = 0.1$ dB is the parameter that, for all practical purposes, represents the system noise figure that is equal to the amplifier noise figure. This can be written as

$$G_A + F' = L_2 + 25.$$

Since $F' = F_A$, the relationship between amplifier gain, amplifier noise figure, and filter insertion loss is

$$G_A = L_2 - F_A + 25. \qquad [29]$$

An entire set of equations can be generated for any allowable difference between system and amplifier noise figure. In general

$$G_A = L_2 - F' + B \qquad [30]$$

where B is the value of $(G_A + F_A)$ at $L_2 = 0$ for any value of $F' - F$.

The region of Fig. 8 in which the $(G_A + F_A)$ curves converge represents an undesirable set of system parameters. In this region, a large change in $(G_A + F_A)$ has a small effect on $(G_A + F')$. Since G_A is the same for both, a large reduction in amplifier noise figure produces a small reduction in system noise figure. This region is characterized by values of filter insertion loss that are large relative to the amplifier gain. To obtain a set of parameters that avoid this region, the filter insertion loss must be reduced or the amplifier gain must be increased. Excellent noise performance can be realized by using parameter values represented by the region of the curve above the straight line corresponding to values of $(F' - F_A) = 0.1$ dB.

It is important to note that system noise performance may not be optimized by simply reducing the amplifier noise figure. Consider a system that has the following parameters.

$$F_A = 20 \text{ dB}$$

$$G_A = 15 \text{ dB}$$

$$L_2 = 10 \text{ dB}$$

The intersection of $L_2 = 10$ dB and $(G_A + F_A) = 35$ dB results in a value of

$$G_A + F' = 35 \text{ at point A of Fig. 8}$$

or a system noise figure of 20 dB. A reduction in amplifier noise figure to 10 dB results in an almost equivalent reduction in F' to 11 dB at point B.

If the amplifier noise figure is reduced to 5 dB, point C is obtained. The system noise figure is 7.5 dB. In going from point B to C, the amplifier noise figure was reduced by 50% with only a 25% improvement

in system noise figure. To achieve greater improvement in system performance requires decreasing the insertion loss, so that point C moves to the left, or increasing the gain so that it moves upward. Both points D and E represent system noise figures of 5.5 dB, i.e., $F' - F_A = 0.5$ dB with $F_A = 5$ dB. Point D is obtained by decreasing the filter insertion loss to 4.2 dB, while point E is obtained by increasing the gain to

$$G_A = (G_A + F') - F'$$

$$= 28 - 5.5 = 22.5 \text{ dB}$$

This improvement in system performance can be achieved by any combination of L_2 and G_A values that are represented by the line $(F' - F_A) = 0.5$ dB and limited by points D and E. $(F' - F_A) = 0.5$ dB rather than 0.1 dB was used because moving point C to the left on the $G_A + F' = 22.2$ dB line would not yield an intersection with $F' - F_A = 0.1$ dB unless L_2 was negative. This would require a reduction of mixer noise figure. In those cases where the post-selector insertion loss is to be reduced, the resonator Q must be inncreased, the image rejection must be decreased or the number of filter sections must be increased. Fig. 3 is used to evaluate the possible tradeoffs. The remaining parameter is the preselector insertion loss. This is simply added to the value determined from Fig. 3 in dB.

$$F'' = F' + L_1 \text{ (dB)} \qquad [31]$$

Application of these graphical procedures to a contemporary electronic tuner results in some interesting observations concerning improvements in performance. The tuner has the following parameters

$G_A = 13$ dB $\quad L_1 = 4$ dB

$F_A = 4.5$ dB $\quad L_2 = 8$ dB

$F_m = 10$ dB $\quad L_s = 48$ dB

$Q_{0c} = 50.$

Fig. 3 gives the system noise figure as $F' = 7.5$ dB. The insertion loss of the preselector must be added to this value to obtain the total noise figure

$$F'' = L_1 + F' = 11.5 \text{ dB}.$$

If the gain of the rf amplifier decreases to 10 dB, as it might well do in production, the total system noise figure increases to 12.8 dB.

Now consider the improvement in system noise figure performance if the total capacitive unloaded Q, Q_{0c}, is increased to 100 and the

image rejection is kept at the same level. Since L_1 is added directly to system noise figure, it is desirable to keep its value as low as possible. An insertion loss of 1 dB will provide an image rejection of 11 dB. The post selector must provide the additional 37 dB of image rejection, which it can do for an insertion loss of 3.7 dB. The value of L_2 to be used in Fig. 3 is

$$L_2' = L_2 + F_m - 8.5 = 5.2 \text{ dB}$$

and

$$F' = 6 \text{ dB}.$$

The resulting system noise figure is

$$F'' = 7 \text{ dB}.$$

If the image rejection of the preselector had been increased to 16 dB the insertion loss would have been 2.1 dB. The insertion loss of the post selector could then have been decreased to 2.5 dB, since only 32 dB of image rejection would have been required. The resulting system noise figure is F'' = 7.7 dB. The 0.7 dB increase is due to the increase in insertion loss of the preselector.

To obtain the same system noise figure by improving amplifier performance rather than increasing the diode Q requires that the noise figure of the amplifier be reduced to 3.0 dB maximum. This value can be determined by considering the fact that the noise figure of the system cannot be better than the noise figure of the amplifier and, since the insertion loss of the preselector is 4 dB,

$$F'' = 7.0 \text{ dB}$$

$$F' = F'' - L_0 = 7 - 4 = 3.0 \text{ dB}$$

To make the system noise figure, F', approximately equal to the amplifier noise figure ($F' - F = 0.1$ dB) requires increasing the amplifier gain to 31.5 dB.

The third option in realizing better system noise performance is to improve the mixer noise figure. Unfortunately, this must still be accompanied by improvements in amplifier or filter performance. For example, if the noise figure of the mixer and i-f were reduced to 0 dB the system noise figure would still be 8 dB due to the insertion loss of both pre- and post selectors.

In addition to improving components to obtain better system performance, trade-offs in filter performance can also be made. If the image rejection of the preselector is allowed to drop to 8.5 dB, the insertion loss is only 1.5 dB. For an image rejection of 26 dB in the post

selector the insertion loss is 3.8 dB. The total image rejection

$$L_s = 34.5 \text{ dB}$$

rather than the original 48 dB. This value can be increased 6 to 10 dB by adding a tracking reject filter as described previously. In this case the system noise figure

$$F'' = 7.7 \text{ dB}$$

which comes very close to the value obtained when the capacitive Q was increased to 100.

Improvements in all these areas will ultimately lead to a system noise figure that is equal to the amplifier noise figure, i.e., 4.5 dB. It is easily seen from the above discussion that the greatest improvement in system noise performance is obtained by decreasing the insertion loss of the pre- and post selectors. This may be accomplished by improving the capacitive unloaded Q or sacrificing image rejection. The decision as to which approach to take can only be reached after careful consideration of cost factors and real system requirements.

Conclusions

The minimum attainable noise figure of a television receiver is the noise figure of the rf amplifier. The ultimate goal is to reduce this to its lowest practical value. The objective of proper system design is to optimize the tuner so that the system noise figure approaches the rf amplifier noise figure. This is accomplished by increasing the gain of the rf amplifier and by decreasing the insertion loss of the pre- and post selectors. The reduction in insertion loss can be accomplished by increasing the unloaded Q of the filter elements or reducing the image rejection. All these tradeoffs can be quickly and precisely determined by use of the derived graphs.

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A COS/MOS Linear Amplifier Stage*

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Abstract—The voltage gain, bandwidth, and noise properties of a COS/MOS-loaded COS/MOS linear amplifier stage are discussed and are compared with those of the simple COS/MOS and MOS-transistor-loaded MOS transistor linear amplifier stages. The voltage gain of this new amplifier stage is independent of the supply voltage and dependent only on the device geometry. This amplifier stage introduces negligible distortion into the signal.

1. Introduction

The amplifier stage discussed consists of two pairs of COS/MOS transistors, as shown in Fig. 1; one pair serves as the amplifying element and the other as the loading element. This amplifier stage can also be considered as a parallel connection of a p-channel and an n-channel MOS-transistor-loaded amplifier stage. The amplifier stage has large controlled voltage gain, large bandwidth, and low noise, and is able to deliver a large amount of current to a load without introducing distortion to the signal. The gain of the amplifier depends only on the geometry of the device used. The input impedance of the amplifier is very large, while its output impedance can be quite small. In conjunction with the voltage amplification feature of MOS transistors, this amplifier stage is excellent for cascade linear integrated amplifier applications.

* The research reported in this paper was sponsored by the Wright Patterson Air Force Base, Dayton, Ohio under contract F33615-73-C-1117.

2. Voltage Gain

The circuit diagram of the amplifier stage is shown in Fig. 1; Q_1 and Q_3 are n-channel and Q_2 and Q_4 are p-channel MOS transistors. The

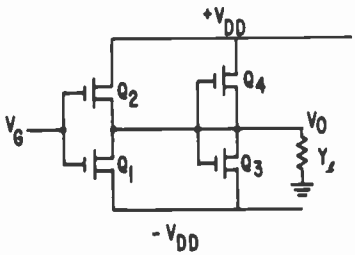

Fig. 1—COS/MOS-loaded COS/MOS amplifier.

current equation for each transistor is given by

$$I_1 = \frac{Z_1}{2L_1}\mu_n C_0(V_G - V_{TN} + V_{DD})^2,$$

$$I_2 = \frac{Z_2}{2L_2}\mu_P C_0(-V_G + V_{DD} + V_{TP})^2,$$

$$I_3 = \frac{Z_3}{2L_3}\mu_n C_0(V_0 - V_{TN} + V_{DD})^2,$$

$$I_4 = \frac{Z_4}{2L_4}\mu_P C_0(-V_0 + V_{DD} + V_{TP})^2. \qquad [1]$$

The current equation at the center node is

$$\frac{Z_1}{2L_1}\mu_n C_0(V_G - V_{TN} + V_{DD})^2 + \frac{Z_3}{2L_3}\mu_n C_0(V_0 + V_{DD} - V_{TN})^2 + V_0 Y_l = \frac{Z_2}{2L_2}\mu_P C_0(V_G + V_{DD} - V_{TP})^2 + \frac{Z_4}{2L_4}\mu_P C_0(V_0 + V_{DD} - V_{TP})^2, \qquad [2]$$

where Y_l is the load admittance. Differentiating Eq. [2] with respect to V_G yields:

$$A_v = \frac{dV_0}{dV_G} =$$

$$\frac{\left[\frac{Z_1}{L_1}\mu_n C_0(V_G + V_{DD} - V_{TN}) + \frac{Z_2}{L_2}\mu_P C_0(V_{DD} - V_G - V_{TP})\right]}{\left[\frac{Z_3}{L_3}\mu_n C_0(V_0 + V_{DD} - V_{TN}) + \frac{Z_4}{L_4}\mu_p C_0(V_{DD} + V_{TP} - V_0)\right] + Y_l}, \quad [3]$$

or

$$A_v = -\frac{g_{m1} + g_{m2}}{g_{m3} + g_{m4} + Y_l'} \quad [3a]$$

where g_{mi} is the transconductance of Q_i. If we assume that the FET's are COS/MOS pairs, that is,

$$\frac{Z_1}{L_1}\mu_n = \frac{Z_2}{L_2}\mu_P \text{ and } \frac{Z_3}{L_3}\mu_n = \frac{Z_4}{L_4}\mu_P, \quad [4]$$

Eq. [3] becomes

$$A_v = -\frac{\frac{Z_1 L_3}{Z_3 L_1}}{1 + \frac{Y_l Z_3}{Z_3(2V_{DD} + V_{TP} - V_{TN})}}. \quad [5]$$

Therefore, if no load is connected to the amplifier, i.e., $Y_l = 0$,

$$A_v = -\frac{Z_1 L_3}{Z_3 L_1} = -\frac{Z_2 L_4}{Z_4 L_2}. \quad [6]$$

The voltage gain of the amplifier stage without load is a function of the geometry of the MOS transistors only. Eq. [5] also shows that for any load admittance, the voltage gain of this amplifier stage is independent of V_G and V_0. This amplifier stage, therefore, introduces no distortion to the signal.

3. Frequency Response

An equivalent circuit of the amplifier stage is shown in Fig. 2. When the amplifier is an intermediate stage, G_l is equal to zero. If the amplifier is an output stage with a pure resistive load, C_{fl1}, C_{fl2}, C_{l1}, and C_{l2} are equal to zero. By inspection, the load admittance, Y_l, is given by

$$Y_l = G_l + j\omega C_{eff}, \quad [7]$$

where

$$C_{eff} = \frac{2 + A_v}{A_v}(C_{f1} + C_{f2}) + \left(1 + \frac{A_v}{2}\right)(C_{fl1} + C_{fl2})$$
$$+ C_{d1} + C_{d2} + C_{g3} + C_{g4} + C_{l1} + C_{l2}. \quad [7a]$$

In this expression C_f is the drain-to-gate capacitance of the MOS transistor. The subscripts d, g, and l correspond to the drain, gate, and load, respectively.

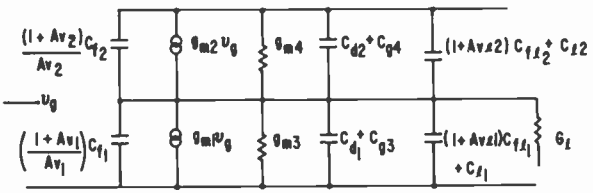

Fig. 2—High-frequency equivalent circuit of COS/MOS amplifier.

The voltage gain of the amplifier stage is, therefore, given by

$$A(\omega) = \frac{-g_{m1}}{g_{m3} + \frac{1}{2}G_l + j\omega C_{eff}/2}. \quad [8]$$

Consequently, the bandwidth of this amplifier, ω_c, is

$$\omega_c = \frac{2g_{m3} + G_l}{C_{eff}}. \quad [9]$$

The gain–bandwidth product, GB, is given by

$$|\mathrm{GB}| = \frac{2g_{m1}}{C_{eff}}. \quad [10]$$

4. Low-Frequency Noise

It can be shown that the low-frequency excess noise, including $1/f$ noise, $g - r$ noise, and trapping noise of an MOS transistor is inversely proportional to the gate area. The low-frequency noise equivalent circuit of a COS/MOS-loaded amplifier stage is given in Fig. 3. From this equivalent circuit, the output short-circuit mean-square noise current is

$$\overline{i^2} = (g_{m1} + g_{m2})^2 \overline{V_g^2} + K\left(\frac{g_{m1}^2}{A_1} + \frac{g_{m3}^2}{A_2} + \frac{g_{m3}^2}{A_3} + \frac{g_{m4}^2}{A_4}\right). \quad [11]$$

The first term on the right-hand side of Eq. [11] is due to the noise source physically located at the gate. The second term is the low-frequency drain excess noise, where K is a constant that depends on the thickness of the gate oxide and the density of surface state, $g - r$, or trap centers. Since the noise source physically located at the gate is

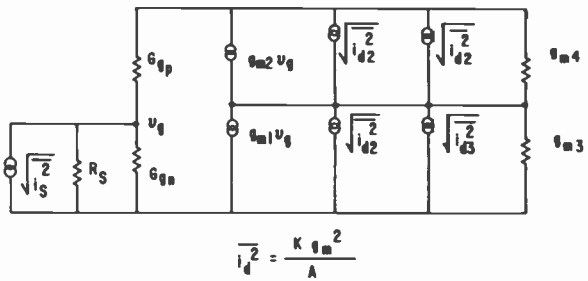

Fig. 3—Low-frequency equivalent circuit.

very small, the equivalent mean-square input noise voltage is given by

$$\overline{V_n^2} = \frac{K}{(g_{m1} + g_{m2})^2}\left[\frac{g_{m1}^2}{A_1} + \frac{g_{m2}^2}{A_2} + \frac{g_{m3}^2}{A_3} + \frac{g_{m4}^2}{A_4}\right]. \qquad [12]$$

If we further assume $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, Eq. [12] becomes

$$\overline{V_n^2} = \frac{K}{4}\left[\frac{1}{A_1}\left\{1 + \frac{1}{A_v}\left(\frac{L_1}{L_3}\right)^2\right\} + \frac{1}{A_2}\left\{1 + \frac{1}{A_v}\left(\frac{L_2}{L_4}\right)^2\right\}\right]. \qquad [13]$$

5. High-Frequency Noise

We now calculate the high-frequency noise of the COS/MOS loaded MOS amplifier stage. The high-frequency limiting noise of an MOS transistor is thermal noise. The mean-square drain noise current, $\overline{i_d^2}$, and mean-square induced gate noise current, $\overline{i_g^2}$, are given, respectively, by

$$\overline{i_d^2} = \alpha \cdot 4kT\, g_{mo}\, \Delta f \qquad [14]$$

and

$$\overline{i_g^2} = \beta \cdot 4kT\, G_{in}\, \Delta f. \qquad [15]$$

Here, $\alpha \simeq \frac{2}{3}$, $\beta \simeq \frac{4}{3}$, g_{mo} is the low-frequency transconduction, and G_{in} is the real part of the input admittance.

The high-frequency noise equivalent circuit of a COS/MOS-loaded amplifier stage is shown in Fig. 4. Assuming that i_s is the thermal noise current of the source resistance, R_s, the noise voltage at the gate is

$$V_g = \frac{i_{g1} + i_{g2} + i_s}{G_s + Y_{g1} + Y_{g2}}. \qquad [16]$$

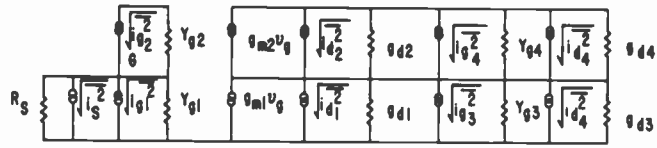

Fig. 4—High-frequency noise equivalent circuit.

The short-circuit output noise current is

$$i_{ns} = V_g(g_{m1} + g_{m2}) + i_{d1} + i_{d2} + i_{d3} + i_{d4}. \qquad [17a]$$

Therefore, the mean-square output noise current is

$$\overline{i_{ns}^2} = K'^2(\overline{i_{g1}^2} + \overline{i_{g2}^2}) + C[K'(\overline{i_{g1}^2} \cdot \overline{i_{g2}^2})^{1/2} + (\overline{i_{g2}^2}\,\overline{i_{d2}^2})^{1/2} + (\overline{i_{g3}^2}\,\overline{i_{d3}^2})^{1/2} + (\overline{i_{g4}^2}\,\overline{i_{d2}^2})^{1/2}] + \overline{i_{d1}^2} + \overline{i_{d2}^2} + \overline{i_{d3}^2} + \overline{i_{d4}^2} + \overline{i_{g3}^2} + \overline{i_{g4}^2}, \qquad [17b]$$

where $K' = (g_{m1} + g_{m2})/(G_s + Y_{g1} + Y_{g2})$ and C is the cross-correlation factor of drain and gate noise. In general, C can be approximated as an imaginary. Its absolute value is approximately equal to 0.4 in MOS transistors. The equivalent input noise voltage is, therefore, given by

$$\overline{V_{eq}^2} = \frac{\overline{i_{g1}^2} + \overline{i_{g2}^2} + \overline{i_s^2}}{(G_x + Y_{g1} + Y_{g2})^2} + \frac{\overline{i_{d1}^2} + \overline{i_{d2}^2} + \overline{i_{d3}^2} + \overline{i_{d4}^2} + \overline{i_{g3}^2} + \overline{i_{g4}^2}}{(g_{m1} + g_{m2})^2}$$

$$+ 2C\left[\frac{(\overline{i_{g1}^2}\,\overline{i_{d1}^2})^{1/2} + (\overline{i_{g2}^2}\,\overline{i_{d2}^2})^{1/2}}{(G_s + Y_{g1} + Y_{g2})(g_{m1} + g_{m2})} + \frac{(\overline{i_{g3}^2}\,\overline{i_{d3}^2})^{1/2} + (\overline{i_{g4}^2}\,\overline{i_{d4}^2})^{1/2}}{(g_{m1} + g_{m2})^2}\right]. \qquad [18]$$

For a simple case, $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $i_{g1} = i_{g2}$, $i_{d1} = i_{d2}$, and the equivalent mean-square input noise voltage is

$$\overline{V_{eq}^2} = \frac{\overline{i_s^2} + \overline{2i_{g1}^2}}{(G_s + 2Y_g)^2} + \frac{\overline{i_{d1}^2} + \overline{i_{d3}^2} + \overline{i_{g3}^2}}{2g_{m1}^2}$$
$$+ C\left[\frac{(\overline{i_{d1}^2}\,\overline{i_{g1}^2})^{1/2}}{g_{m1}(G_s + 2Y_{g1})} + \frac{(\overline{i_{g3}^2}\,\overline{i_{d3}^2})^{1/2}}{2g_{m1}^2}\right]. \qquad [19]$$

Substituting Eqs. [14] and [15] into Eq. [19] and assuming that the circuit is properly tuned, the equivalent input mean-square noise voltage is

$$V_{eq}^2 = \left\{\frac{G_s + 2\beta G_{g1}}{(G_s + 2G_{g1})^2} + \frac{\alpha(g_{m10} + g_{m30}) + \beta G_{g3}}{2g_{m1}^2}\right.$$
$$\left. + 2C\left[\frac{\sqrt{G_{g1}g_{m10}}}{g_{m1}(G_s + 2G_{g1})} + \frac{\sqrt{G_{g3}g_{m30}}}{2g_{m1}^2}\right]\right\} 4kT\Delta f. \qquad [20]$$

where G_{g1} and G_{g3} are the real parts of the input conductance of MOS transistors Q_1 and Q_3, respectively.

6. Experiments

A CD4007A, dual COS/MOS plus inverter, was chosen to demonstrate the loading effect on the distortion of the amplifier. For a sim-

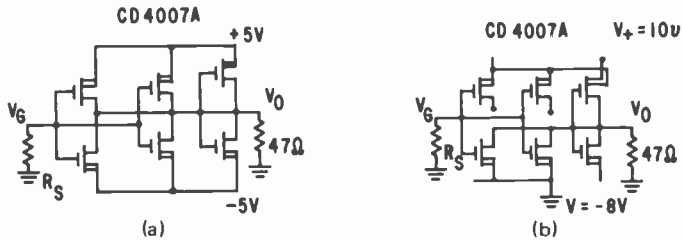

Fig. 5—(a) CD4007A connected as COS/MOS-loaded COS/MOS amplifier and (b) CD4007A connected as simple MOS-transistor-loaded MOS transistor amplifier.

ple transistor-loaded MOS amplifier, the two n-channel MOS transistors of the COS/MOS pair were connected in parallel with the p-channel MOS transistor of the inverter as the load. For a COS/MOS amplifier, the two COS/MOS stages were connected in parallel and the gate of the inverter was connected to its drain electrodes as a load. These circuit configurations are shown in Fig. 5. The source resistance in both cases is 600 ohms. With these arrangements, Z_a is equal to $2Z_l$ and L_a is equal to L_l in both configurations, where Z and

Table 1—Distortion of the Output Signal, CD4007A Connected as a Transistor-Loaded Amplifier Stage

10 kHz	2nd Harmonic (20 kHz)	3rd Harmonic (30 kHz)
30 mV	−30 dB	. . .
100 mV	−20 dB	−50 dB

L are the channel width and channel length of the MOS transistors, respectively, and the subscripts a and l represent the active and load MOS transistors. When the CD4007A was connected as a simple transistor-loaded MOS transistor amplifier, the supply voltage was adjusted to obtain the optimum operating condition. When the circuit was connected as a COS/MOS amplifier, the supply voltage was arbitrarily set to ±5 V. The operating frequency was chosen to be 10 kHz. If the load resistance is 10 megohms, the voltage gain for the transistor-loaded and COS/MOS amplifier stages was found to be 1.24 and 1.95, respectively, compared with $\sqrt{2}$ and 2 as predicted by the simple theory. For the distortion measurement, the load resistance was set at 47 ohms. The experimental results are shown in Tables 1 and 2. Table 1 shows that there is a large distortion when the CD4007A is connected as a simple transistor-loaded amplifier. Table 2 shows that when the same unit of CD4007A is connected as a COS/MOS amplifier, the distortion of the amplifier is not significant.

Eq. [3] shows that the sum of g_{m3} and g_{m4} is independent of V_G and V_0. Therefore, Q_3 and Q_4 may be replaced by two resistors without introducing distortion to the signal. However, under this condition, the voltage gain is given by

$$A_v = -\frac{Z_l \mu_n C_0 (2V_{DD} + V_{TP} - V_{TN})}{L_l G_l}. \qquad [21]$$

This voltage gain increases with the supply voltage, as illustrated in Fig. 6. The voltage gain is plotted as a function of bias voltage for a COS/MOS-loaded and a resistor-loaded COS/MOS amplifier stage constructed by using the same type CD4007A device. This experiment confirms that for a COS/MOS-loaded stage, the voltage gain is

Table 2—Distortion of the Output Signal, CD4007A Connected as a COS/MOS Loaded Amplifier Stage

10 kHz	2nd Harmonic (20 kHz)	3rd Harmonic (30 kHz)
30 mV	−72 dB	. . .
100 mV	−65 dB	. . .
300 mV	−62 dB	. . .

independent of bias voltage and that the voltage gain of a resistor-loaded stage increases with bias voltage. The simple theory expects the gain of the resistor-loaded stage to increase linearly with supply voltage. The measured voltage gain increases monotonically with supply voltage. The linear relationship between voltage gain and supply voltage was not observed, however. Presumably this is due to the hot current carrier effect. At larger gate-to-source bias voltages, the elec-

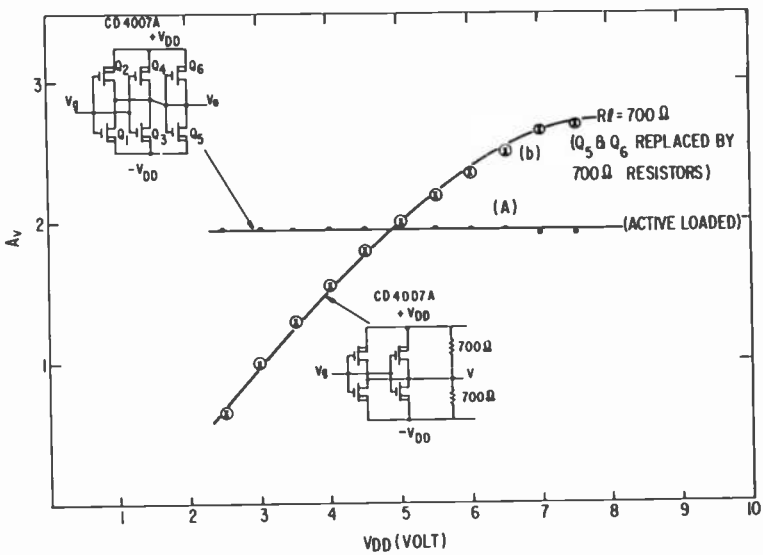

Fig. 6—Voltage gain versus supply voltage for COS/MOS-loaded amplifier stage and resistor-loaded COS/MOS amplifier stage.

tric field intensity at the inversion layer is large, and the carrier mobility decreases. Hence, the voltage gain decreases with the increasing supply voltage.

The dependence of voltage gain on frequency for bulk and for SOS MOS transistors is shown in Figs. 7 and 8, respectively. The bulk device is a CD4007A while the SOS device is a developmental type having the same transistor configuration as that of CD4007A. Both figures show the voltage gain versus frequency of a simple COS/MOS stage, a COS/MOS-loaded COS/MOS amplifier stage as in Fig. 5a, and an MOS-transistor-loaded amplifier stage as in Fig. 5b. The supply voltage in all cases is ±5 V. As shown in Fig. 7, the CD4007A inverter has a low-frequency voltage gain of 29 and a 3-dB bandwidth of 3.1 MHz. The gain–bandwidth product is equal to 90 MHz. The

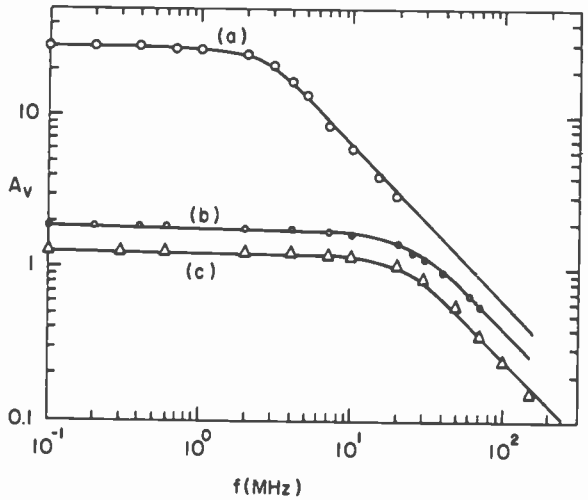

Fig. 7—Frequency dependence of CD4007A bulk MOS amplifiers: curve (a) is for a simple COS/MOS inverter; curve (b) is for a COS/MOS-loaded COS/MOS amplifier; and curve (c) is for an MOS-transistor-loaded amplifier.

new amplifier stage has low-frequency gain of 1.9 and the 3 dB bandwidth of that stage is equal to 25 MHz. The gain–bandwidth product of this stage is only about one half that of the single inverter. This is presumable due to the interaction among the MOS transistors. As shown in Fig. 8, the gain–bandwidth product of the SOS/COS/MOS inverter and the SOS/COS/MOS-loaded COS/MOS amplifier stage are approximately the same. The interactions between SOS/MOS

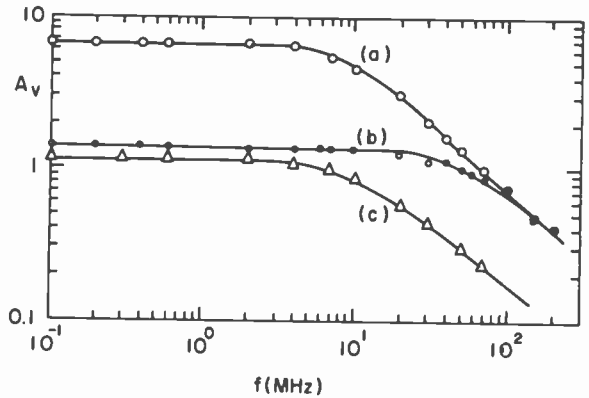

Fig. 8—Same set of curves as in Fig. 7, but for amplifiers using SOS/MOS developmental type having the same transistor configuration as the CD4007A.

transistors are negligibly small. The MOS-transistor-loaded amplifier stage has lower voltage gain. The bandwidth of the MOS-transistor-loaded stage is approximately the same as the COS/MOS-loaded COS/MOS amplifier stage. The low-frequency voltage gain of the SOS version of COS/MOS inverter, COS/MOS-loaded COS/MOS amplifier stage, and MOS-transistor-loaded amplifier stage are 6.6, 1.4, and 1.15, respectively. This small voltage gain is caused by the large drain output conductance of SOS MOS transistors. The drain conductance acts as a load to the amplifier which in turn, reduces the voltage gain as is shown by Eq. [3]. If the MOS transistors are not truly complementary and the threshold voltages of the n-channel and the p-channel devices are not equal, the voltage gains of the COS/MOS-loaded COS/MOS stage and the MOS-transistor-loaded amplifier stage can be significantly different from those predicted by the simple theory. Since the transconductance increases with the supply voltage, the bandwidth of all three of these types of amplifier stages increases with the supply voltage.

7. Discussion

The performance of a COS/MOS-loaded MOS amplifier stage has been demonstrated. We compare the performance of this amplifier with the simple COS/MOS amplifier and the simple active loaded MOS amplifier configurations.

The voltage gain of this amplifier stage is smaller than that of a simple COS/MOS amplifier stage. This is because the COS/MOS-loaded stage has a large output conductance. The output conductance of a simple COS/MOS amplifier is equal to the sum of the drain conductances of the MOS transistors used, while that of the COS/MOS-loaded stage is equal to the sum of the transconductance of the load COS/MOS pair and the drain conductance of the active COS/MOS pair. From Eq. [3] the voltage gain of a simple COS/MOS amplifier is

$$A_v = \frac{-\left[\frac{Z_1}{L_1}\mu_n C_0(V_{DD} + V_G - V_{TN}) + \frac{Z_2}{L_2}\mu_P C_0(V_{DD} + V_{TP} - V_G)\right]}{g_{d1} + g_{d2} + Y_l}. \quad [22]$$

This voltage gain increases with the supply voltage. If this amplifier is an intermediate stage, $Y_l = 0$, the voltage gain is inversely proportional to the drain conductance of the MOS transistors. On the other hand, the voltage gain of the COS/MOS-loaded MOS amplifier stage is controlled by the device geometry of the transistors used.

From Eqs. [7] to [10], it is clearly seen that the output capacitance of the COS/MOS-loaded MOS amplifier is slightly larger and the output conductance is much larger than those of the simple COS/MOS amplifier stage. As a result, the COS/MOS-loaded amplifier has a larger bandwidth. The gain–bandwidth products of these two types of COS/MOS amplifiers are comparable, however.

It can be easily shown that at low frequencies

$$\overline{V_n^2}\Big|_{mod} = \overline{V_n^2}\Big|_{simp} + \frac{K}{4A_v}\left[\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_2}{L_4}\right)^2\right], \qquad [23]$$

and at high frequencies

$$\overline{V_{eq}^2}\Big|_{mod} = \overline{V_{eq}^2}\Big|_{simp} + \frac{\alpha g_{m30} + \beta G_{g3} + C\sqrt{G_{g3}g_{m30}}}{2{g_{m1}}^2}. \qquad [24]$$

Here the subscripts *mod* and *simp* represent the corresponding values for the COS/MOS-loaded and the simple COS/MOS amplifier stages, respectively. The last terms in Eqs. [23] and [24] are due to Q_3 and Q_4. These two terms are much smaller than the other terms in the equations. No significant difference in noise property is expected from these two types of amplifier stages.

The voltage gain of the COS/MOS-loaded amplifier stage is equal to the square of that of an MOS-transistor-loaded MOS amplifier. From Eq. [7a] we see that C_{fl1} and C_{fl2} are small. The effective capacitance, C_{eff}, of the COS/MOS-loaded amplifier stage is approximately two times that of an MOS-transistor-loaded amplifier stage, assuming the same active and load transistors are used. The bandwidths of these two types of amplifiers are approximately equal. The gain–bandwidth product of the COS/MOS-loaded amplifier is, therefore, larger than that of MOS-loaded amplifier stages by a factor equal to the voltage gain of the MOS-loaded amplifier.

It can be shown that the low-frequency excess noise of an MOS-transistor-loaded amplifier stage is

$$\overline{V_n^2} = \frac{K}{A}\left[1 + \frac{L_1}{L_2}\right]^2, \qquad [25]$$

where A is the gate area of the active transistor, K is the same constant as in Eq. [11], and L_1 and L_2 are the lengths of the gate of the active and the load transistors, respectively. The high-frequency noise of this amplifier stage is

$$\overline{V_{eq}^2} = \left[\frac{G_s + \beta G_{g1}}{(G_s + G_{g1})^2} + \frac{\alpha(g_{m10} + g_{m20}) + \beta G_{g2}}{g_{m1}^2} \right.$$

$$\left. + 2C \left\{ \frac{\sqrt{G_{g1} g_{m10}}}{(G_s + G_{g1}) g_{m1}} + \frac{\sqrt{G_{g2} g_{m20}}}{g_{m1}^2} \right\} \right] \cdot 4kT\Delta f. \qquad [26]$$

From Eqs. [25] and [26] and Eqs. [12] and [19], it is seen that the noise performance of the COS/MOS-loaded amplifier stage is much better than that of an MOS-transistor-loaded amplifier stage. However, the most significant advantages of COS/MOS-loaded amplifier stages are larger bias-independent voltage gain, large gain–bandwidth product, large dynamic range, and capability of delivering large current to a load without introducing distortion to the signal. This amplifier stage with voltage gain slightly less than unity has been used in the COS/MOS standard cells for linear, threshold, and programmed logic array applications. The amplifier stage also has been used for TV signal processing and the amplification of the output signal of CCD's and surface-wave devices.

Acknowledgment:

The author wishes to thank R. G. Coalter for many valuable discussions.

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J. J. Amodei and W. Phillips Crystals for Recording Phase Holograms (3,915,549)
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W. H. Barkow Waveform Generating Circuit (3,911,295)
C. D. Boltz, Jr. Timing Signals for Velocity Error Correction (3,914,542)
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G. W. Carter and S. E. Hilliker Electromagnetic Radiation Filter for Coaxially Fed Hot Chassis Television Receiver (3,913,038)
B. M. Childers and C. Fesperman, Jr. Dyeing Station in an Apparatus for Continuously Dyeing Fibrous Material (3,913,359)
R. J. Clark High-Resolution Digital Generator of Graphic Symbols with Edging (3,918,039)
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Cheng P. Wen received the B.S., M.S., and Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1956, 1957, and 1963, respectively. From 1956 to 1963 he was employed by the Electron Physics Laboratory of the University of Michigan working on traveling-wave amplifiers and electron beam noise problems. In March 1963 he joined RCA Laboratories, Princeton, N. J., where he has worked on ultra-low-noise microwave amplifiers, gas lasers, microwave acoustics, ferromagnetic semiconductors, microwave magnetics in integrated circuits, and millimeter-wave avalanche diodes. He joined Science Center, Rockwell International, in March 1974.

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STATEMENT OF OWNERSHIP

Statement of Ownership, Management and Circulation (Act of October 23, 1962, Section 4369, Title 39, United States Code.)

1. Date of filing: September 25, 1975. 2. Title of publication: RCA REVIEW. Frequency of issue: Quarterly. 4. Location of known office of publication: RCA Laboratories, Princeton, New Jersey, 08540. 5. Location of headquarters or general business offices of the publishers: RCA Laboratories, Princeton, New Jersey, 08540. 6. Names and address of publisher and editor: Publisher, RCA Laboratories, Princeton, New Jersey, 08540. Editor, Ralph F. Ciafone, RCA Laboratories, Princeton, New Jersery, 08540. 7. Owner: RCA Corporation, 30 Rockefeller Plaza, New York, New York 10020; Cede & Company, Box 20, Bowling Green Stn., New York, New York 10004; Merrill, Lynch, Pierce, Fenner & Smith, Inc., 70 Pine Street, New York, New York 10005; Cudd & Company, C/o Chase Manhattan Bank, Box 1508 Church Street Station, New York, New York 10008; Martin B. Seretean, C/o Coronet Industries, Box 1248, Dalton, Georgia 30720; Tnom & Company, Box 577, Central Station, St. Louis, Missouri 63188.

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